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Minimizing Clock Skew During Place & Route

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Meeting timing constraints at P&R for designs running near 600-700 MHz is a problem when the design has tight skew constraints. This article discusses a quick-fix that proved useful recently to minimize skew and simultaneously meet the required timings in a 650Mhz design.

The designer used CTGen, a clock tree synthesis tool from Cadence Design Systems, Inc.

CTGen traces through the clock tree and generates a clock tree topology by removing / inserting buffers and inverters and defining their levels that best satisfies user-specified delay and skew constraints in the CTGen constraints file. This occurs for any Input pins not declared as CLK pins in the file containing timing information for Library cells (TLF file).

The original clock tree is shown in Fig. 1, while the corresponding CTGen constraints file is shown in Fig 2.

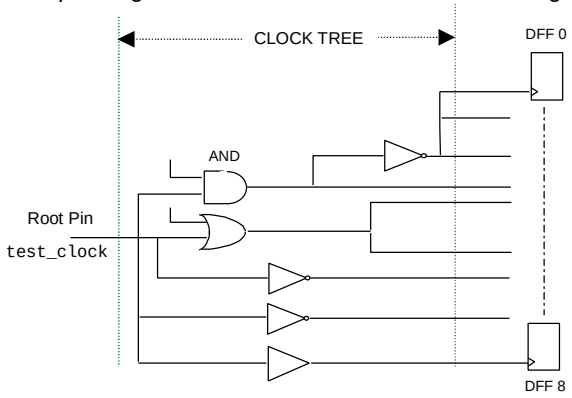


Fig. 1

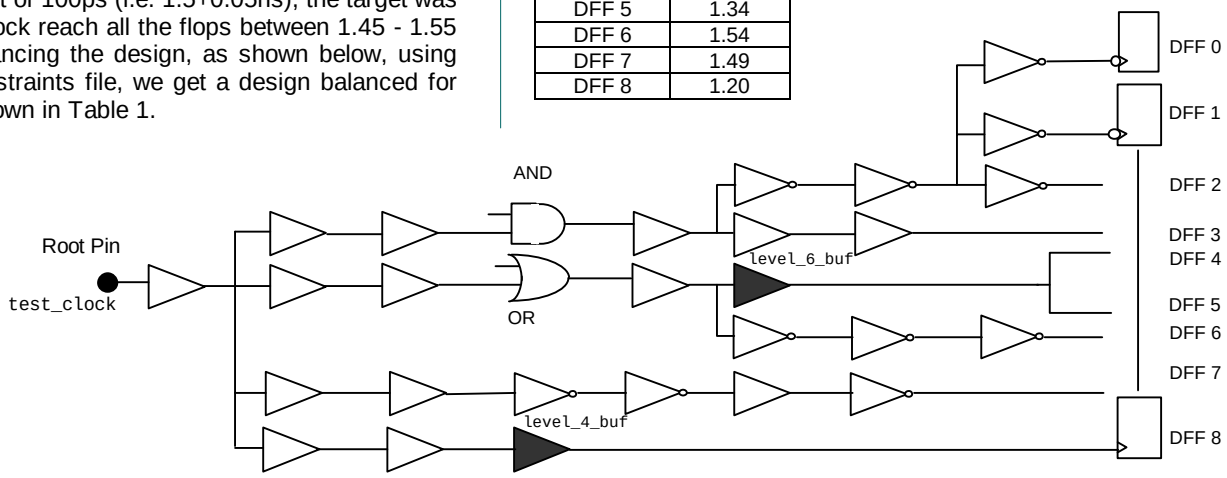
```
specify_tree
        root_iopin      'test_clock'
leaf_pins
        'AND'           'b' rising
        'OR'          'b' rising

set_constraints
        waveform          0.5 5.0 0.5 5.0
        min_delay         1.45
        max_delay         1.55
        max_skew          0.09
        max_transition    0.3
define_cells
buffers 'buf_s_1' 'buf_s_2' 'buf_s_3' 'buf_s_4' 'buf_s_5'
inverters 'inv_s_1' 'inv_s_2' 'inv_s_3' 'inv_s_4' 'buf_s_5'
-----------------------------------------------
specify_tree
        root_pin          'AND'   'x'
set_constraints
        waveform          0.5 5.0 0.5 5.0
        min_delay         1.00
        max_delay         1.02
        max_skew          0.01
        max_transition    0.3
define_cells
buffers  'buf_s_1' 'buf_s_2' 'buf_s_3' 'buf_s_4' 'buf_s_5'
inverters 'inv_s_1' 'inv_s_2' 'inv_s_3' 'inv_s_4' 'buf_s_5'
-----------------------------------------------
specify_tree
        root_pin          'OR'    'x'
set_constraints
        waveform          0.5 5.0 0.5 5.0
        min_delay         1.00
        max_delay         1.02
        max_skew          0.01
        max_transition    0.3
define_cells
```

The design having been targeted for a 1.5ns clock with skew constraint of 100ps (i.e. 1.5+0.05ns), the target was to make the clock reach all the flops between 1.45 - 1.55 ns. After balancing the design, as shown below, using the above constraints file, we get a design balanced for the timings shown in Table 1.

Table 1

FLOPS	Timing (ns)
DFF 0	1.45
DFF 1	1.53
DFF 2	1.51
DFF 3	1.48
DFF 4	1.31
DFF 5	1.34
DFF 6	1.54
DFF 7	1.49
DFF 8	1.20



As can be seen: Skew (Max insertion delay - Min insertion delay) of 340ps, which is clearly unacceptable.

Since, most of the paths are balanced, running the clock synthesis tool again for unbalanced paths would mean risking changing the timings for the already balanced paths. To avoid doing this we calculate the time difference required to make the unbalanced paths fall within the required insertion delay gap and then balance those paths again, using a different constraints file as shown in Fig. 3

Here, rather than disturb the whole balanced tree, the unbalanced paths from the last buffer attached to the flops 4,5 & 8, have been balanced, with the output pins of the buffers shaded black (see Fig. 4) being considered as root pins. This balances the unbalanced paths by inserting more buffers or inverters (shaded gray) after the root pins only. The final balanced clock tree is shown in Fig. 4. ■

```
specify_tree
        root_pin          'level_6_buf'   'x'
set_constraints
        waveform           0.5 5.0 0.5 5.0
        min_delay          0.15
        max_delay          0.20
        max_skew           0.03
        max_transition     0.3
define_cells
buffers  'buf_s_1' 'buf_s_2' 'buf_s_3' 'buf_s_4' 'buf_s_5'
inverters 'inv_s_1' 'inv_s_2' 'inv_s_3' 'inv_s_4' 'buf_s_5'
-----------------------------------------------------------
specify_tree
        root_pin          'level_4_buf'   'x'
set_constraints
        waveform           0.5 5.0 0.5 5.0
        min_delay          0.25
        max_delay          0.30
        max_skew           0.03
        max_transition     0.3
define_cells
buffers  'buf_s_1' 'buf_s_2' 'buf_s_3' 'buf_s_4' 'buf_s_5'
inverters 'inv_s_1' 'inv_s_2' 'inv_s_3' 'inv_s_4' 'buf_s_5'
```

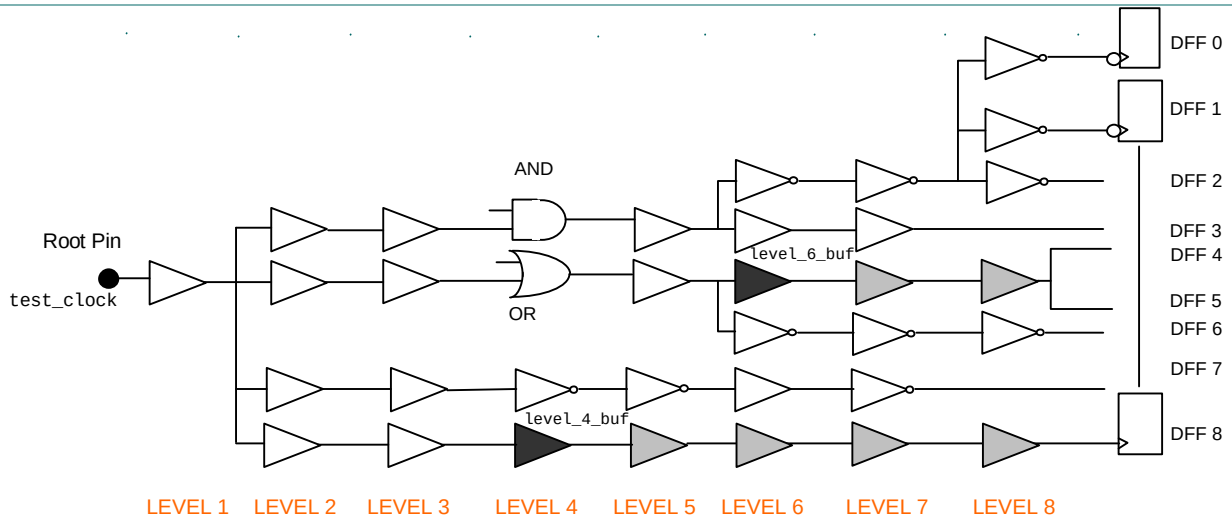


Fig. 4