Design Advantage™
We build them for YOU.℠
Comit Systems, Inc. Newsletter
Volume 3 Number 1 Jan. – Feb. 2000

Verilog® Coding Tip for Easy Visual Verification

During simulation, we often require to observe different combinatorial states of several signals which, when taken together, are of significance to the desired operation of the design.

Using meaningful ASCII names for the different combinatorial states (instead of hexadecimal or binary values), as labels, can be helpful in observing groups of signals and their correlation with logical states or operations that they initiate or signify.

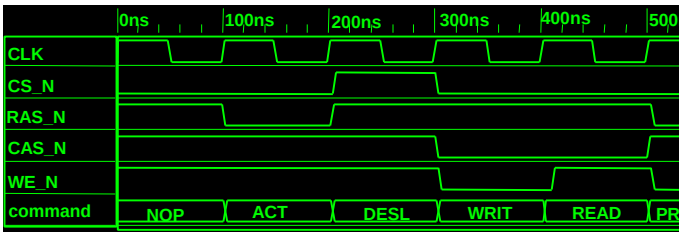
The concept is illustrated below, through an example from the verification suite of a SDRAM controller. The SDRAM receives various commands via the control bus. These commands are made up of various combinations of four control signals. If observed separately in a simulation browser, it can require considerable effort to relate the various combinations of the states of the signals to particular commands. In the code fragment below, meaningful ASCII names have been assigned to the various combinatorial states:

```
reg  [(4*8)-1:0]   command;

// Declaration of a variable to
// display 4 characters. This
// variable is used to observe the
// command bus.


// definitions to observe commands on
// SDRAM command bus


// Command Truth table
// {CS_N, RAS_N, CAS_N, WE_N}


`define DESL 4'b1111
`define NOP  4'b0111
`define READ 4'b0101
`define WRIT 4'b0100
`define ACT  4'b0011
`define PRE  4'b0010
`define PALL 4'b0010
`define CBR  4'b0001
`define MRS  4'b0000
```

```
// The following code is added in the
// test-bench to display the command
// string in the simulation browser

  always @(CS_N or RAS_N or CAS_N or WE_N)

begin

      case ({CS_N, RAS_N,  CAS_N, WE_N})
          `DESL : command <= "DESL";
          `NOP  : command <= "NOP ";
          `READ : command <= "READ";
          `WRIT : command <= "WRIT";
          `ACT  : command <= "ACT ";
          `PRE  : command <= "PRE ";
          `PALL : command <= "PALL";
          `CBR  : command <= "CBR ";
          `MRS  : command <= "MRS ";
        default: command <= "UNDF";
      endcase
  end
```

[Note: If this code is added in the RTL file, then proper synthesis pragmas need to be added, as the code is not synthesizable]

The diagram below shows the four control signals and the commands corresponding to their various combinatorial states being executed, in the simulation browser.



Meaningful ASCII names in the simulation browser help in debugging the design, since bus operations, current state of state machine, and the group of signals can be correlated easily.

Free HDL Quick Reference Card Offer

If you program in VHDL or Verilog®, you can send in for your very own free copy of a Quick Reference Card of your favorite HDL. Attractively produced in Coated Text Gloss, these handy trifolds offer a convenient alternative to referring a Language Reference Manual. To receive your free copy in the mail, simply send e-mail to FreeQRC@comit.com, with your mailing address and the quantities of each QRC you require.

Offer valid till supplies last.

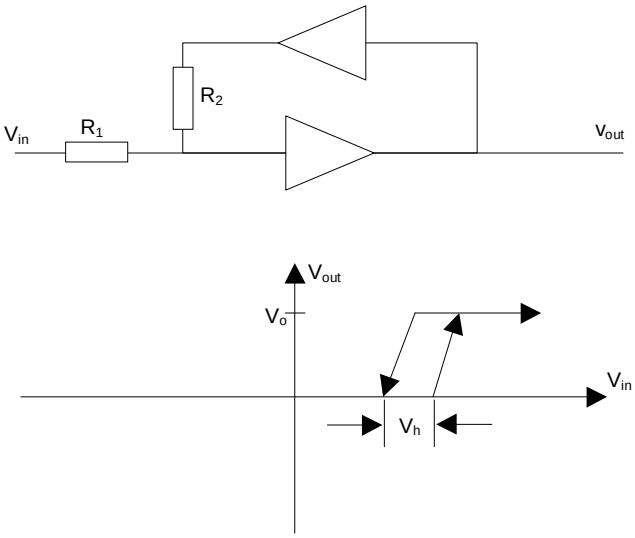
Hurry! Quantities limited!

Digital Schmitt Trigger

By K. Radhakrishnan

When slow rising/falling signals in a noisy environment pass through ordinary buffers, there can be glitches at the buffer outputs as the signal varies around the buffer's input threshold. Hence the buffer output cannot be directly fed to a latch, nor can it be used as a clock to a flip-flop.

One solution is to use Schmitt buffers with hysterisis at their inputs. The addition of hysterisis can sharpen the input signal. Most often, this necessitates the use of additional buffer chips on board. The circuit on the right shows how buffers in existing logic circuits (PALs, FPGAs, PLDs etc), can be used to add hysterisis to the input gate. This increases the noise threshold of the circuit considerably, while avoiding additional chip count on the board.



In the News

Comit Signs Japanese Alliance Partner

Offers Precision Miniature PCB Design & Manufacturing.

Marking a strategic initiative in its Japanese operations, Comit has established an alliance with Apollo Giken of Yokohama. Apollo Giken will market Comit's services in the areas of ASIC Design & Verification, FPGA Design and Embedded Systems Design to its customers in Japan. Apollo Giken provides Digital / Analog Circuit Design, miniature PCB design & manufacturing and industrial design, primarily to the Matsushita Group and Sony Corporation.

The alliance also provides Comit with access to high precision miniature circuit board design and manufacturing facilities to augment its service offerings to its US and European customers. Further details are available at www.comit.com under News & Events.

Lucent Technologies signs ORCA™ series FPGA design order with Comit

Lucent Technologies recently signed a design order on the ORCA™ series FPGA, with Comit.

The design, to be executed at Comit's Global Design Center in Santa Clara, includes integration of Comit's own and 3rd party IP cores, and is being implemented using Lucent's ORCA™ Foundry 9.4 software.