esign Advantage™

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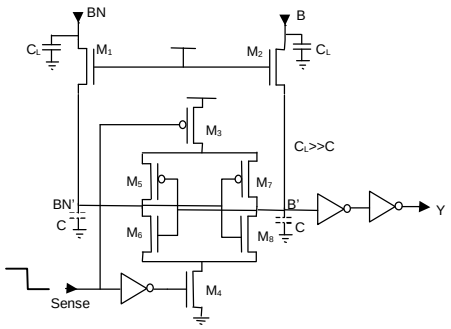
Design Advantage

Low Voltage Fast Differential Sense Amplifier

By Tapan Samaddar

Designing low power memories with small access times is a circuit design challenge, particularly where a small differential voltage needs to be measured at low supply voltage in order to determine the state of a cell.

The figure below shows a circuit for an ultrafast differential sense amplifier implemented for low voltage applications (Vdd = 1.2volts) whose sensitivity is augmented by the addition of two transistors implemented as voltage dependent resistors.

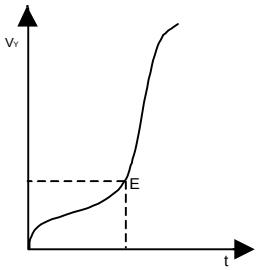


Nodes B and BN are differential nodes and are connected to the memory cell element or any differential voltage source whose voltage needs to be amplified fast. The capacitances associated with the nodes B and BN are very high, while capacitances of the nodes B' and BN' are very low.

The circuit shows transistors M5, M6 and M7, M8 connected as a crossed coupled latch, whose sizing is such that their gain-bandwidth (GBW) product in the metastable condition is maximum. Also, transistors M1, M2 have Vdd applied to their gates which biases them in saturation, and hence they offer a very low resistance path between the nodes B-B' and BN-BN'.

Normally the "sense" terminal is high and so the latch is off. Whenever a difference voltage is applied to nodes B and BN and "sense" terminal is pulsed low the circuit operation starts and the cross coupled latch goes into metastable state. As soon as the differential signal appears across the cross coupled latch, positive feedback will amplify the difference signal, and the voltage at nodes B' or BN' will start rising.

Two factors helps in making this circuit response very fast: The rising voltage at node B' or BN' causes the gate to source voltage across transistors M1 and M2 to decrease, which causes their channel resistance to increase.



This process isolates the nodes B-B' and BN-BN'. Since the capacitances associated with nodes B' and BN' are extremely small, the voltage rise is exponential, which in turn helps to turn off M1 and M2.

The graph shows the output response of this circuit. The point E denotes the time when transistors M1, M2 turn off which in turn causes a rapid rise in output voltage.

This circuit was implemented in silicon with 0.25 micron technology, and yielded worst case sense time of less than 1.7ns. ■

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