Design Advantage™

The newsletter of:

COMIT® SYSTEMS

Comit Systems, Inc.
3375 Scott Blvd. Suite 330
Santa Clara, CA 95054
Phone : (408)-988-7966

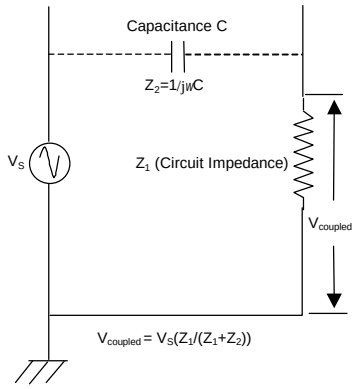
Editor : Jaishankar Iyer
We welcome your comments and suggestions. Please email us at jiyer@comit.com

Minimizing Stray Capacitance and Parasitic Coupling Effects

By Tapan Samaddar

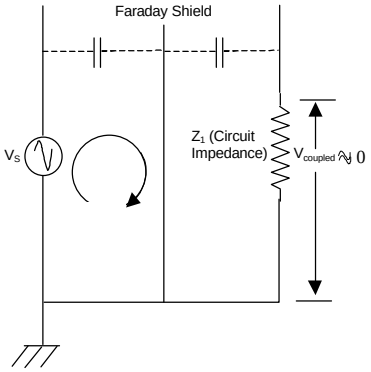
Stray Capacitance occurs whenever two current carrying conductors are in close proximity, especially if they are parallel to each other. Stray capacitance commonly occurs between parallel traces on a Printed Circuit Board (PCB) or between traces/planes on opposite sides of a PCB.

The occurrence and effects of stray capacitance are, unfortunately, often overlooked during circuit modeling and can lead to serious performance problems, especially at high frequencies, when the system circuit board is constructed and assembled. Examples of problems include increased noise, reduced frequency response, and even, circuit instability. The figure below shows a parasitic coupling effect with a ac noise source Vs.



If the capacitance formula is applied to the case of wire traces on opposite sides of a PCB, then for general purpose PCB material (permitivity, ER = 4.7; separation, d = 1.5 mm), the capacitance between conductors on opposite sides of the board is just under 3pF/cm^2. At a frequency of 250 MHz, 3pF corresponds to a reactance of 212.2 ohms.

Stray capacitance cannot be completely eliminated. Certain design measures, however, can be taken to reduce it. One solution is to use a Faraday Shield, which is simply a grounded conductor between the coupling source and the affected circuit.



As shown here, implementation of a Faraday shield interrupts the coupling electric field. Notice how the shield causes the noise and coupling currents to return to their source without flowing through Z1.

Taking care of issues like this up-front in the design cycle can save expensive redesign and rework in later stages of product development.