Design Advantage™
The newsletter of Comit Systems, Inc.
Volume 1, Issue 1 June 1998

Architecture Optimization Helps Speed Up Design 5x

Recently Comit Systems was called upon to design a Finite Impulse Response filter for a certain FPGA architecture. Initial trials with RTL design showed that the performance of the filter was rather dismal, and it was left to us to see how we could improve upon this. We studied the FPGA carefully, and came up with a design strategy optimized for the technology. This strategy provided a fivefold increase in performance over the initial results.

Choosing the right FIR filter was the first step to tuning performance. We separately evaluated several different FIR filters based on how optimally the target technology would support each. The second step was to choose a multiplier which would work well with the selected FIR design. We evaluated four different alternatives i.e., the Booth multiplier, the Simple Tree, the Wallace Tree and ADA and concluded that a handcrafted Wallace Tree with a fourteen level pipeline results in the fastest performance. We similarly wrote four level pipelined adders etc. in VHDL, and synthesized the design with Synopsys. The end result was a FIR filter speeded up five times which used every feature of the target technology possible for the design.

With this project we demonstrated that achieving very high speed designs using a HDLA methodology requires careful optimization of the ■

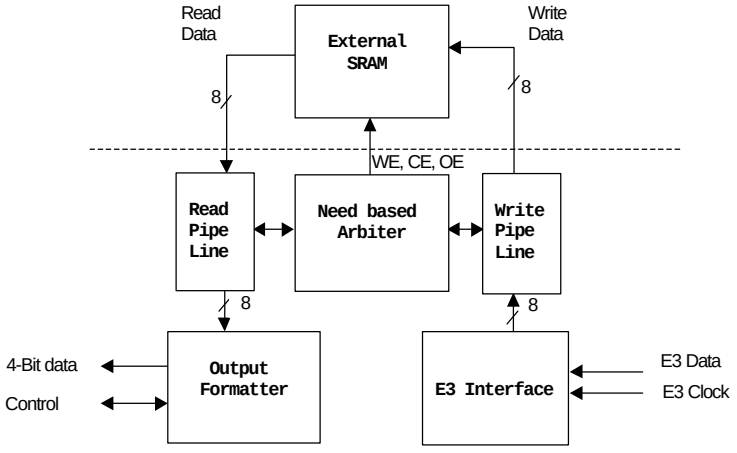

Fig. 1: Need based arbitration scheme keeps read pipeline full, write pipeline empty.

Innovative Arbitration Scheme Between Two Different Clock Domains

A common requirement for telecom network applications is maintaining a continuous datapath across different clock domains. Usually this is done with FIFO memories with different read and write clocks. In our case, the design did not lend itself to FIFO manipulation. This called for alternative methods to make the design workable. Comit used a simple 8K static RAM to achieve the same effect, thus cutting cost and obviating the need to redesign boards. This ensured quicker product turnaround.

We considered several issues during the design and did calculations for the minimum depth of the SRAM, the minumum pipe length and the maximum allowable frequency error and so on. We arrived at figures that would tolerate the allowable drifts with ease. The design was coded in VHDL and synthesized using Synplicity.

Our design is outlined in Fig. 1. The incoming serial data was from a E3 telecom line at 34.368 MHz and the outgoing data was 4-bit wide at 16.736 MHz. The design consisted of a serial to 8-bit parallel convertor, which extracted bytes from the E3 frame and stored them in a write pipeline. Another module was designed to format data from a read pipeline and send out data in the required 4-bit format. We designed an arbitration scheme which would ensure data integrity while reading and writing. This called for a 4 byte pipeline for both operations. The uniqueness of the arbiter was that it monitored the pipe status on either side and drained or filled the pipes on a need-to basis rather than having a request-grant algorithm. Thus, the arbiter always managed itself so as to keep the write pipeline empty and the read pipeline full. The arbiter dynamically decided the priority to meet this goal. It was determined that with the request-grant mechanism, the accumulated delay could cause data to be dropped, hence this approach to the arbiter.

We eliminated the need for FIFOs which may have called for a board redesign by using an innovative arbitration scheme between two clock domains. ■

Design Advantage™

The newsletter of:

COMIT® SYSTEMS

Comit Systems Inc.
3375 Scott Blvd. Suite 330
Santa Clara, CA 95054

Download White Paper on Engineering Outsourcing:

http://www.comit.com

Chips, Boards, Systems and Software Design

"Comit Systems responded impressively to our urgent request and put in countless hours even on evenings and weekends to get our project well accomplished on time. We know we can certainly count on Comit Systems for their flexibility, versatility, and superior work quality. "Thank you, Comit, for your commitment to your customers."

Thomas Au
VP of Engineering,
Turner Designs.

In this inaugural issue of our newsletter, we would first like to thank all of our customers.

We achieved several important milestones this past year. Comit is now the exclusive Design Center for Marshall Industries nationwide. We are also the first Synopsys Certified Design Center in the West Coast, for Cell Based Array (CBA) technology.

We are the exclusive design center for Marshall Indus-

These partnerships are a further validation of our business model as a unique vendor neutral Engineering Outsourcing Service Provider (OSP).

We continue to invest in our Design Center. Located in a 4000 s.ft facility in the heart of Silicon Valley, with over $1M worth of equipment and tools installed, Comit can handle several large projects simultaneously, in these key areas:

- ASIC Front-end design
- ASIC Verification and Back-end
- FPGA design
- EDA Software development
- Embedded Systems development
- Windows drivers and firmware development

We are the first certified Synopsys CBA design center in the West Coast.

In our newsletters, we will share with you some of the design tricks that saved time and money for our custmers, and other technical information of general interest to the designers. ■

Did You Know? Comit Systems Inc. Also Designs Embedded Systems.