Prof. Marteean of Nafromere says Contract Engineering will save Silicon Valley

Doom and gloom in Silicon Valley, but there was a lone sane voice. In a well-attended lecture, the noted Professor Marteean, Professor of The Business of Technology, University of Nafromere, talked to big-wigs, money-bags, CEOs and VPs of engineering of several high, low and medium profile start-ups and established companies.

Attendees were looking for wisdom, or something, or anything that would give them a clue as to what to do to go forward from here.

Prof. Marteean did not mince words. He said, "Your problem appears crystal clear: Start-ups are renting office space, putting up cubes, hiring people, buying systems and tools, trying to build teams, prove processes… which can take years anyway, and established companies are constantly re-tooling against rapid obsolescence. Remember, the mission is to build products. Go build them quickly, using Contract Engineering."

A member of the audience asked, "But Professor, we have a Not-Invented-Here policy in our company, to reject good ideas."

The Professor responded, "Madam, Contract Engineering is invented *right here* in Silicon Valley. Only I am from Nafromere."

http://www.comit.com/contract-engineering

Prof. Marteean's Tech Notes

What does this piece of Verilog code do?
Can you make it shorter?

```
integer i;

wire    [31:0]  din;
reg     [31:0]  dout;

always @(din)
begin
   dout[31] <= din[31];
   for (i = 0; i < 31; i = i + 1)
   begin
      dout[i] <= din[i+1] ^ din[i];
   end
end
```

Answers at http://www.comit.com/technotes

Verilog & VHDL Quick Reference Cards are now available for download to PDA!
www.comit.com

COMIT® SYSTEMS
The Contract Engineering Company
3375 Scott Blvd Ste 330
Santa Clara CA 95054
USA
(408) 988 2988

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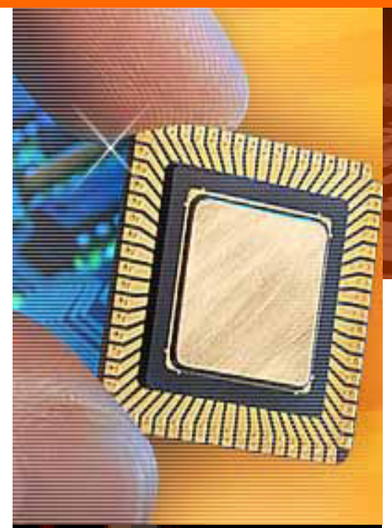


0.13 micron SoC Taped Out

Comit recently taped out of a **multi-million gate SoC to TSMC 0.13 micron** process. The design included an embedded processor core and 17 clock domains, with some of the internal logic running at upwards of 620 MHz. Comit implemented the design jointly with the customer and alliance partner eSilicon, to deliver a DRC-clean GDSII.

This positions Comit among the handful with proven multi-million gate complex SoC experience in 130 nanometer technology.

Comit joins UMC ASICplus™ Program

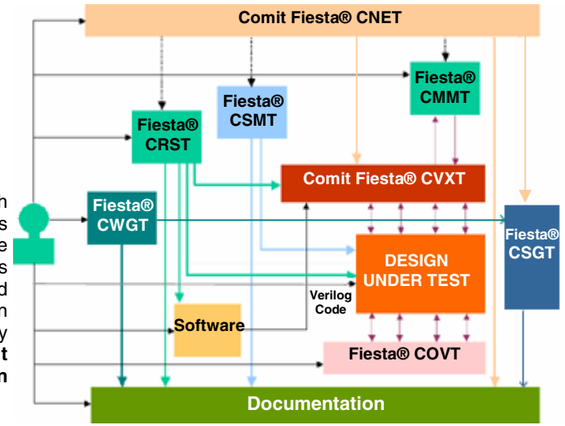
Comit signed a technology alliance partnership agreement with United Microelectronics Corp. (UMC), joining its ASICplus™ Partners program.

The partnership will enable Comit to gain early insight into UMC technologies and their best fit to Comit customers' projects.

UMC is a leading semiconductor foundry that manufactures advanced process ICs for applications spanning major sectors of the semiconductor industry. UMC delivers cutting-edge foundry technologies that enable sophisticated system-on-chip (SOC) designs, including 0.13 micron copper/low k, embedded DRAM, and mixed signal/RFCMOS. In addition, UMC is a leader in 300mm manufacturing.

Introducing Fiesta®

Comit's Process Standardization and Acceleration Toolkit.



In an initiative to share with customers the many process enhancement techniques that have been the foundation of Comit's reputation for delivering reliable and accurate designs on time and within budget, Comit's Methodology Consulting Group released the **Comit Fiesta® Process Standardization and Acceleration Toolkit.**

Targeted to design teams building multi-million gate ASICs and complex SoCs, Fiesta® is an industrial-strength suite of tools designed, developed, tested and used by engineers of Comit Contract Engineering Center. The toolkit addresses key design and verification issues to get designs up and running early with a high confidence level, and coexists with industry standard EDA tools.

>> Details inside

Enterprise Level Contract Engineering

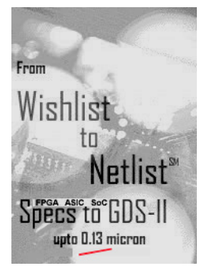
Unprecedented flexibility. Better ROI

Comit now offers enterprise-level Contract Engineering.

Comit works with companies developing electronic products: conducting resource audits and determining a comprehensive range of engineering services required to address their product development roadmap. Contract Engineering offers flexibility through access to truly scalable engineering resources, and better ROI by converting fixed costs of design, development and test engineering to variable ones.

Specs to GDSII under one roof

Avanti® flow for backend



With the establishment of the Avanti® flow for backend services, Comit now offers complete specs-to-GDSII solutions under one roof.

Comit backend services were recently used in conjunction with Comit front-end services to deliver a multi-million gate complex SoC in TSMC 0.13 micron process.

Fiesta® shaves months off complex SoC design

Comit recently completed a complex SoC design. The success and speed of implementation of the design were significantly influenced by the use of tools from the Fiesta® Process Standardization and Acceleration Toolkit.

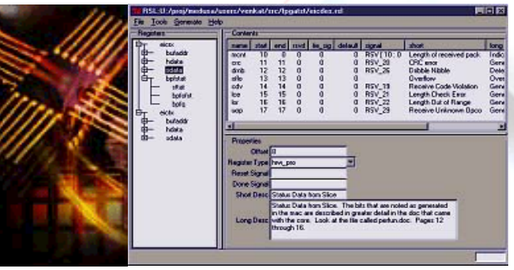
Venkat Iyer, Sr. Director of Engineering at Comit, who led the project said, “Right from the micro-architecture stage we saved months and brought in tremendous discipline by using Fiesta® CRST. Throughout the project we used CRST to automatically propagate spec changes to all generated outputs ensuring consistency and reducing errors.

We simultaneously used CMMT to generate simulation time memory models that were used in advanced system-level verification. This enabled us to focus on the real business of implementing intent driven logic.”

More on Fiesta® ...

CRST Register Specification Tool

CRST is a register specification and change management tool. Manual definition of register specifications is time consuming and error-prone. Specification changes introduce further delays and increase the probability of errors due to the need for rewriting Verilog® code and redoing documentation. Propagation of changes is hard to track manually. CRST addresses all these issues. It aids design implementation by automating the specification of registers. It automatically generates the necessary synthesizable Verilog code, verification definitions that plug into Fiesta® Open Verification Environment, C headers and documentation, dramatically speeding up design, verification and software development cycles and updating documentation, all at one go. Device driver development can start as soon as the first cut register specification is done, allowing for early feedback loops.



CSMT Finite State Machine Editor

CSMT is a graphical editor for finite state machines. This tool saves time by allowing rapid and easy definition of state machines and automatically generating Verilog® code and documentation. The tool provides a Graphical User Interface (GUI) that lets users add states, transitions, expressions, input and output signals to a state machine. The GUI provides easy drawing of state machine diagrams.

CVXT Open Verification Environment

CVXT is a complete Open Verification Environment. It saves time by allowing rapid and painless implementation of module-interactive system level testing that is difficult to do in Verilog or C. Commonly available alternatives for system-level verification require the designer to master an additional or proprietary syntax or language. In CVXT, tests are specified in Tcl using a set of just 12 commands.

The CVXT Verification Engine provides the needed interactivity between tests and models to simulate a real-world environment. CVXT offers the ability to build parallel, automated, synchronized self-checking verification testbenches for complex ASIC, SoC and programmable SoC designs. The environment bolts on to industry standard Verilog simulators and supports both real-world system testing and rigorous hardware module level and interface tests. The user can either run system level code intended for final silicon to test functionality, or do feature-by-feature self-checking of the chip modules, in parallel and in simultaneous interaction with other modules in the design.

CMMT Simulation Memory Modeler

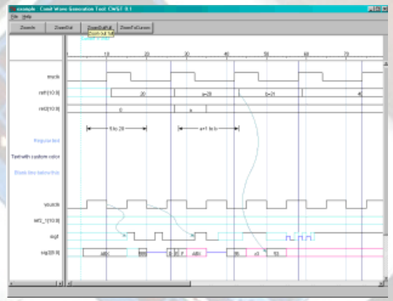
CMMT is a tool to generate simulation time memory models that can be used in advanced system-level verification. CMMT can generate memories with built-in high-level task-definitions to facilitate access from CVXT Open Verification Environment or standalone Tcl test cases to set up and read data in blocks. CMMT can configure memory models to any size. Width and depth are dynamically changeable at run time. Memory models generated can be used in test environments involving many interfaces like Ethernet, Voice (SCC), ADSL, HPNA, USB and their peripheral models in a test environment.

CNET Architectural Code Generation Tool

CNET accepts block level architectural input including third party IP and generates implementation roadmap by defining placeholders for all modules and interfaces.

CWGT Waveform & Constraints Generation Tool

CWGT saves time by quickly generating signal behavioral depictions with highlighted dependencies and timings from a set of just six commands. With more embedded information than capturing screen-shots, CWGT is particularly useful in situations such as design document creation where waveform cause-effect relationships need to be understood by a group well before the final code can be ready. CWGT outputs can be directly used to update timing constraints in CSGT synthesis script generator.



CSGT Synthesis Script Generation Tool

CSGT accepts constraints and generates scripts to automate synthesis flow for popular synthesis tools.

Fiesta® Process Standardization and Acceleration Toolkit is an industrial-strength suite of tools designed, developed, tested and used by engineers of Comit Contract Engineering Center. Their experience in developing processes and methodology that yield predictable and accurate results forms the foundation of the toolkit. Use it with confidence. Additional integration and support services, if desired, are available from Comit.

For downloadable brochures, visit:
http://www.comit.com/products/products.htm

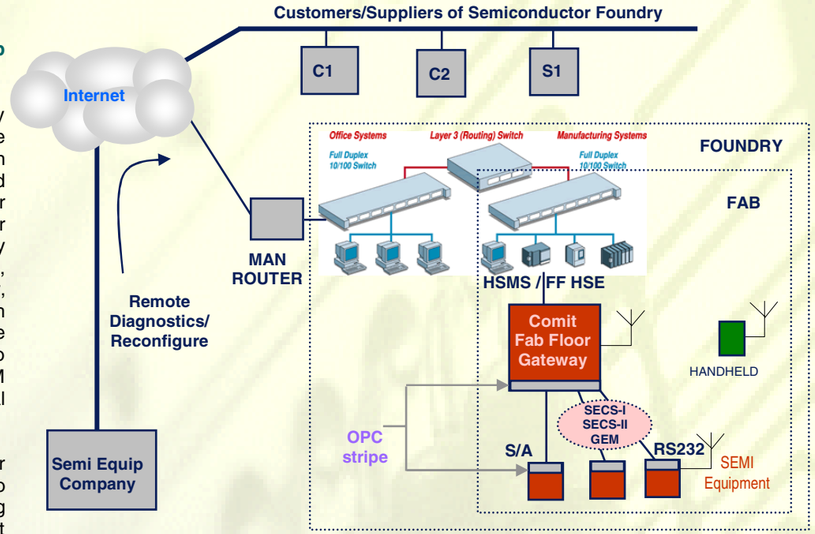
Fab Floor Gateway Solution

Enabling enterprise IT connectivity to fab floors and factory equipment

Comit offers a Customizable Fab-floor Gateway Architecture solution that provides enterprise side connectivity to fab floors through a Foundation Fieldbus HSE interface carrying data, voice and video over TCP/IP, and running seamlessly over commercial Ethernet. Dedicated controllers for different protocols provide fab floor connectivity for Wireless Ethernet, Foundation Fieldbus H1, video on demand through the 1394 controller, and support for legacy serial I/O through aggregation onto a USB device controller. The architecture is capable of customization to support sensor/actuators, SECS-I, SECS-II, GEM and HSMS standards, etc. and non-fab industrial equipment as well.

The software strategy utilizes the OPC (OLE for Process Control) extensions integrated into commercially available Real Time Operating Systems (RTOS) to integrate inter-equipment connectivity with enterprise applications while addressing reliability, availability, serviceability, and security (RASS) requirements.

The Customizable Fab-floor Gateway Architecture combines Comit’s experience in building multi-protocol gateways in multi-million gate ASICs and FPGAs, and our understanding of the real-time software issues that need to be addressed to establish communication amongst legacy-interface equipment.



MoSys and Comit Ink Partnership Alliance

High density, high speed, low cost, low power memory benefits SoC customers

Monolithic System Technology, Inc., (“MoSys”) develops, licenses and markets innovative memory technology for semiconductors. MoSys' patented 1T-SRAM® technology offers a combination of high density, high speed, low cost, and low power consumption unmatched by other memory technologies. 1T-SRAM memories are available as licensable intellectual property to designers who want to efficiently embed large memories in their system-on-chip designs as well as in stand-alone memory devices from MoSys.

Comit recently signed an alliance partnership agreement with MoSys.

UMC Technology Forum

Attracts Enthusiastic Audience. Shows Uptick in Design Activity.

Comit participated in the Partners’ Pavilion of the UMC Technology Forum organized by United Microelectronics Corp. at the Santa Clara Convention Center on June 7, 2002. Increased booth traffic indicated uptick in new design starts and increased interest in contract engineering.

Comit 10th Anniversary

On the occasion of its 10th Anniversary, Comit hosted a reception for customers, partners and associates at The Triton Museum of Art in Santa Clara on February 19, 2002.