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Volume 5 Number 2 Mar-Apr 2002

High Frequency Board Layout and Design, in Multiprocessor Environments

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High frequency board design has always been a challenge in multi-processor environments.

The latest DSP processors in the market, from companies like Texas Instruments, Analog Devices etc, have made the bandwidth requirements for audio synthesis, speech recognition, video processing and many other similar signal processing applications achievable. Many systems, which are based on these processors, need multiple processors on board to handle different tasks and to meet application bandwidth requirement. These processors share resources like, on board memories, PCI Bridge, arbitration logic, perhaps FPGAs implementing data processing engines and input and output devices for accepting audio and video, etc.

With advanced techniques like signal integrity study and SPICE simulations, today boards can be designed with very high accuracy and studied for their performance before they are actually manufactured. Even then, it is a challenge to meet all the performance metrics of a design and get quick closure on functional as well as timing requirements. This creates a requirement on logic designers and PCB designers to start with a correct board layout topology, to avoid changes down the road and increase the probability of meeting design performance metrics.

Comit has extensive experience in high frequency board design in complex environments, and we tend to follow some basic rules during the design and board layout phases of a product.

We list here some tips that can increase the probability of early closure on board layout projects and, hopefully, help you reduce the “Time to Market” for your products.

Stack: Let us consider an eight-layer board, which is a very common case nowadays. Stack should be so designed as to have balanced power & impedance layers. Depending on where power layers are laid in the stack, different signal layers will have different impedances, e.g. in the example stack below, signal layers #1 & #6, signal layers #2 & #5, signal layers #3 & #4 will have the same impedance. Based on design requirements, more power stacks can be added.

Design tips:

1. Route all clocks and critical signals near power planes so that radiation and cross-talk problems can be minimized
2. Terminate all clocks with appropriate series resistors; place these series resistors close to the clock source
3. While routing any signal if the trace has to be switched between layers, use another signal layer in the same pair, e.g. use layer #3 and #4, #2 and #5 to switch the signal on these layers
4. Pin escapes should be as close as possible to their respective devices
5. Tightly daisy chain address and data bus for all the devices
6. Avoid long stubs (branches) on the address and data lines to avoid large reflection on these traces
7. Route clocks in star fashion; match the trace length of clock signals going to each device
8. Route address & data bus and control signals on layer #3 and #4, equidistant from power for an equal impedance pair of planes
9. Lower order address bus switches at higher frequency than the higher order bus; therefore, as far as possible while routing the address bus on board put low order bus bits on the inner side of the bus and put higher order bus bits on the outer edge of the bus
10. Low order address bus bits should have greater separation between them, compared to that between high order bus bits
11. Separate clock signals from each other as much as possible
12. All signals routed on the same layer, as the clock, should be completely separated from the clock signals
13. If there are devices operating at different power supply voltages power plane should be carefully cut: signals traveling between devices operating at different supply voltages should not cross the power plane cuts
14. If there are multiple supply voltages and a power plane cut is necessary, cut the respective ground planes in a way that signals won’t cross the power cuts

15. Physical connections between these different grounds on board (necessitated by the power and ground plane cuts requirement) should be made close to the power supply connection and not just anywhere on the board
16. If there is a central arbitration unit on the board or even if individual processor has inbuilt arbitration logic, match the Bus Request and Bus Grant signal trace lengths accurately
17. As far as possible match the Address and Data bus and control signal trace lengths. If that is not possible because of routing density the Address and Data bus should have less skew than the control signals
18. If signals are crossing two boards via a connector, both the boards should have the same characteristics of impedance
19. Signals coming from (as well going out to) the external world on board should be should be terminated at the connector to avoid radiation
20. Try and run as few signal traces as possible on the top and the bottom layer of the board.

There are many other factors, which contribute to a healthy board. Noise radiation, susceptance, design and application requirements need to be studied carefully to determine what other precautions may be required. However, if the above-mentioned techniques are adopted, they can substantially increase the reliability of board bring up and production. ■

Comit Completes OC48-UTOPIA L3 Design Using Xilinx® Virtex™-II Pro.

Exercises IBM PPC405, Multipliers and Rocket I/O™

Comit is pleased to announce completion of an OC48 to UTOPIA L3 Interface Bridge design on the Xilinx Virtex-II Pro Platform FPGA. OC48 (2.5 Gbps) full duplex serial backplane interfaces were provided through Xilinx Rocket I/O™ transceivers.

Parallel and serial loopback in hardware was controlled by Virtex-II Pro's embedded IBM® PPC405 D5 RISC CPU, using the PPC DCR interface. The PPC405 incorporates the IBM CoreConnect™ architecture implementation of the Processor Local Bus (PLB), Onchip Peripheral Bus (OPB) and DCR.

In a separate design Comit interfaced its FFT and DDR controller IP cores to the PPC405 PLB and exercised the multipliers in the Virtex-II Pro device.

Comit is a Xilinx Xperts Partner. Comit is also an IBM CoreConnect licensee.

Comit joins ARM® Technology Access Program (ATAP®)

Becomes ARM Approved Design Center

The ATAP program provides a framework for selecting and enabling competent design centers with the ARM technology necessary for system-on-chip (SoC) designs.

Speaking at a reception on the occasion of Comit's 10th Anniversary, Chris Russo, Networking Segment Sales Manager for ARM said, "Comit has specific expertise in large SoC designs incorporating ARM processors. Comit is active in the areas of wired and wireless networking, digital imaging, storage area networks and handheld consumer applications. Comit's extensive experience in designing chips, boards and embedded software uniquely positions them to deliver complete system solutions. We are pleased to welcome Comit into the ATAP program as an ARM Approved Design Center."

More info at: www.comit.com

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