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Volume 4 Number 6 Nov-Dec 2001

An Introduction to the Verification Process

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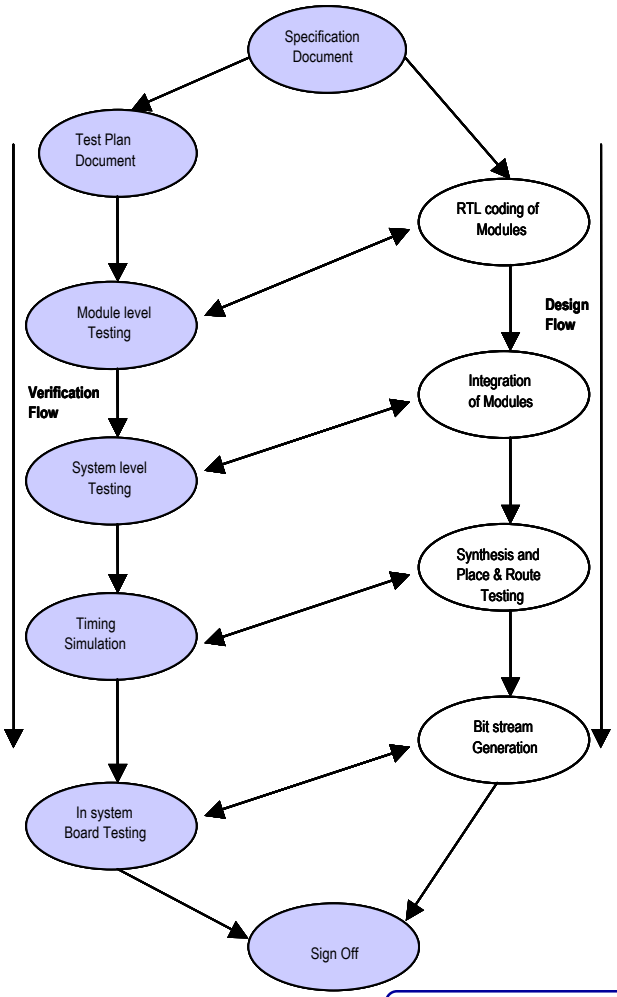
As design complexity increases, new strategies have to be adopted for verification and test to preserve design quality. Designers can benefit from a carefully defined and executed verification plan that takes into consideration all the critical issues involved in the design. Though it is often mentioned as very important, verification remains the underdog, and less process driven.

Verification is a strategy to make sure all functions of the design meets the specification document. Verification is not simulation. Simulation is a tool that is used in the verification effort. The steps typically involved in test and verification are as follows:

- Specification
- Verification Test Plan
- Simulation and System tests
- In-System tests
- Hand off.



Specification

Specification is the basis for the test plan. The specification document explains all the interfaces, features to be used and the overall functionality of the system except the implementation details. With a complete specification document, all test cases that are required to validate the system can be identified. With the information on test cases available, the resources that are required for the verification effort can be identified.

The suitability of the architecture for verification is also addressed here. Changes to the architecture to aid verification will reduce verification and debug time.

Verification Test Plan

A test plan should be developed in order to define the testing strategy. The test plan is developed from the specification. The verification strategy should ensure system functionality and system performance. The design and verification teams should be working from the same completed specification. The levels of tests to be done are outlined at coverage, protocol, interfaces and timing levels. The functions of each interface or block are identified. The conditions of when an expected response occurs are described in the specification. A determination of the number of test benches needed, their complexity, and test module dependencies are made to ensure that the test bench verifies all the modules.

The test plan should identify the following:

a) Tools – Tools required for the verification effort
b) External Models – The need for external stimuli or response and the need for simulation models. Simulation models may be available for some devices that are connected to the chip or system
c) Functions that can be tested using simulation and those functions that can be tested in system (on board)
d) Estimate of the overall schedule for the verification effort.

All tests should be self checking. The test system needs to be scalable to support multiple tests, and be configurable, so that any subset of tests can be run.

Simulation and System Tests

The next step involves test bench coding. This may involve coding of simulation models to model an external device that is connected to the system. Care should be taken to ensure that the simulation model interface that interfaces with the design meets the interface specification. The test bench should generate test vectors for each module under the design. The verification strategy should also address reuse of the block level tests at the system level.

Verification may involve multiple coding languages (like C, Tcl and Verilog®), provided by multiple vendors. HDL Test benches can be written using behavioral constructs. The behavioral test bench allows the designer to simulate the RTL until it meets the functionality specified in the test plan. Once validated, the RTL is ready for synthesis.

For complex designs, code coverage tests help avoid major bugs at an early stage. Coverage tests involve measuring statement coverage, toggle coverage, and state machine tests. Code coverage does not prove functional correctness. The outputs of the simulation should be examined and/or self-testing test benches be used in conjunction with code coverage to ensure complete functionality of the module. In complex systems, it is a good practice to develop an automated test bench, where the stimuli generated by the test bench and the required response can be programmed in a simulation script file.

The same behavioral test bench is used to simulate the design after synthesis and Place and Route. At the interface where the simulation models interface to the design, care should be taken that the stimuli generated by the test bench meets the timing (setup and hold times) required at the chip input pins. The results of the gate level simulation are compared to the RTL simulation output to ensure that the design still meets the functions specified in the test plan.

In this process some bugs may be found, which have to be reported to the design team. The design team will do the bug fixes, and these steps will iterate till the design meets all the functionality listed in the test plan.

In-System Test

In-system testing of the design on board is critical. Even if the design passed the tests in timing simulation, it may not work on board. This is because the board may have variations in timing and electrical characteristics from those modeled in the simulation. In the case of ASIC designs, DFT (Design For Testability) needs to be implemented in the design to enable the testing of system functionality on board. In case of FPGA designs, the fact that FPGAs are re-programmable, eases the In-system tests.

Hand Off

Hand off can occur when the design on board meets all the features listed in the test plan.

Conclusion

Staying in lock-step with the design process is the only way to get your verification done in time. Verification strategy affects architecture: provisioning is needed to make verification easier, and the system easier to debug. Plan, estimate and allocate resources and time up front for verification. Always have a metric to measure verification progress. ■

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