UART 16550 COMPATIBLE MACRO

Product Description 1.0

Features

- Fully Programmable Baud Rate Generator
- Fully Programmable Transmission Interface. 5-,6-,7- or 8 bit character's
- Even / Odd, Stick Parity or No Parity Generation
- One or Two Stop Bits
- In the FIFO mode transmitter and receiver are each buffered with 16 byte FIFOs
- DMA signaling is available through two pins TXRDY_L and RXRDY_L.
- Indepedent receiver clock input
- False start bit detection
- Line Break Generation and Detection
- Status reporting capabilies
- Independently controlled transmit,receive,line status and data interrupts
- Modem control functions [CTS, RTS, DSR, DTR, RI, DCD]
- Supports fully prioritized Interrupt Control System
- Easy interface to microprocessors

Facts
UART 16550 Compatible Macro

Core Specifics		
	XC4010XL	
CLBs Used	383	
IOBs Used	42	
Serial Clock	Upto 10 MHZ	
Supported Devices		
	I/O	CLBs
XC4010XL PC84	40	163
Design Tool Requirements		
Xilinx Core Tools	M1 1.4	
Entry/Verification Tools	ModelTech	
Synthesis Tools	Synplicity Synplify	

Potential Applications

RS232 Communications
Serial Interface to Microcontrollers
Serial Interface to LCD controller
Modem Interface

Recommended Design Experience

Knowledge of Asynchronous Communication. Familiarity with HDL design Methodology in a hierarchical design environment.

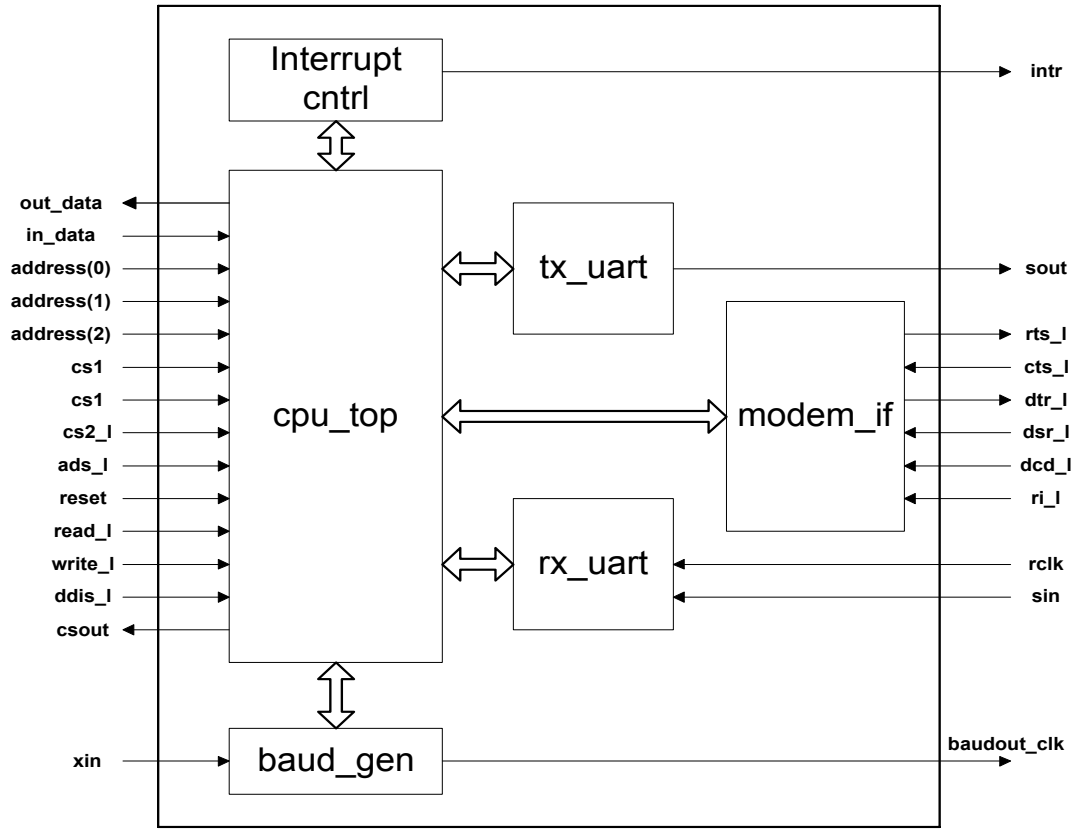

Figure 1. 16550 Compatible UART Block Diagram

General Description

The UART Macro is divided in six submodules. Each can be optimized depending upon the target application. The CPU interface can be optimized depending upon the type of microcontroller interface required.

Functional Description

Cpu_top Module

This module interfaces to parallel bus/ microcontroller and generates chipselects and read/write signals for internal UART registers. This module can be customized to any asynchronous/synchronous bus interface.

Tx_uart Module

This Module converts parallel data to serial according to the serial format programmed in the LCR register and transmits over a serial line.

Rx_uart Module

This module receives serial data and converts it to parallel data. The data received is stored in the buffer. In 16550 mode the rx_uart module can buffer upto 16 bytes of the data. The FIFO size is programmable and can be increased for maximum throughput.

Modem_if module

This module provides interface to modem signals.

Baud_gen module

The baud_gen module generates the required baud for transmitting the data.

Core Modifications

The 16550 compatible macro core design is modular, making modifications is relatively simple. If you are interested in obtaining a version of the core that is different from this product description, then contact Comit Systems directly. Comit Systems can provide custom version of core, including the

changes in microprocessor interface, changes in line interface and adding the additional features required.

Pinouts

The pinout of the UART has not been fixed to specific FPGA I/O allowing flexibility with user application. The signal names are provided in the Table 1 below.

Signal Name	Type	Description
Reset	Input	Global reset signal
Address	Input	Address lines. address(0), address(1) and address(2) are three inputs used during Read rd_l and Write wr_l operations to read from or write into to select the ACE register [from internal Register Bank] .
In_data	Input	in_data(7-0) and out_data(7-0) are the unidirectional input and output data lines that provide out_data(7-0) a bidirectional path for data, control and status information between the ACE and the CPU.
ads_l	Input	Address Strobe. The positive edge of the ads_l signal latches the ACE Register select (address 0 - 2) and Chip Select (cs0,cs1,cs2_l) signals
Read_l	Input	When read_l is low while the core is read_l Input selected, the CPU can read status information or data from the selected UART registers [register bank].
write_l	Input	When write_l is low while the core is write_l Input selected, the CPU can write control words or data into the selected UART registers [register bank].
cs0	Input	Output to the tx_uart block which indicates that transmitter holding register is full.
cs1	Input	Chip Select. When cs0 , cs1 are high and cs2_l low , the ACE is selected.
cs2_l	Input	Chip Select. When cs0 , cs1 are high and cs2_l low , the ACE is selected.
cts_l	Input	cts_l is a modem status signal. Its condition can be checked by reading bit 4 of the modem status register. Bit 0 of the modem status cts_l . Input register indicates that this signal had changed state since the last read from the modem status register. It the modemstatus interrupt is enabled when cts_l changes state, an interrupt is generated.
Dcd_l	Input	dcd_l is a modem status signal. Its condition can be checked by reading bit 7 of the modem status register. Bit 3 of the modem status register indicates that this signal had changed state since the last read from the modem status register. It the modemstatus interrupt is enabled when dcd_l changes state, an interrupt is generated.
ddis_l	Input	when the CPU is not reading data. This output can be used to disable the drivers.
Dsr_l	Output	dsr_l is a modem status signal. Its condition can be checked by reading bit 5 of the modem status register. Bit 1 of the modem status register indicates that this signal had changed state since the last read from the modem status register. It the modem status interrupt is enabled when dsr_l changes state, an interrupt is generated.
Dtr_l	Output	Data terminal ready. When asserted, dtr_l informs a modem or a data set that the ACE is ready to establish communication. dtr_l is placed in active state by setting DTR bit of the modem control register to a high level. dtr_l is deasserted by clearing DTR bit of the modem control register.
Out_data	Output	in_data(7-0) and out_data(7-0) are the unidirectional input and output data lines that provide out_data(7-0) a bidirectional path for data, control and status information between the ACE and the CPU.
Intr	Output	This pin goes high when whenever any one of the following interrupt types has an active high condition and is enabled via the IER. Receiver Error Flag, Received Data Available, Transmitter Holding Register Empty, and Modem Status. The INTR signal is reset low upon the appropriate interrupt service or a Master Reset Operation.
Rclk	Input	Receive Clock. This input is the 16 X baud rate clock for the receiver section of the chip.
Ri_l	Input	When low this indicates that the telephone ringing signal has been received by the Modem. The ri_l signal is a Modem Status input whose condition can be tested by the CPU reading bit 6(RI) of the Modem Status Register. Bit 6 is the compliment of the ri_l signal. Bit 2 of the Modem Status Register indicates whether the

Signal Name	Type	Description
		ri_l input signal has changed from a low to a high state since the previous reading of the Modem Status Register.
Rts_l	Input	Request to Send. When low this informs the Modem or Data Set that the UART is ready to exchange data. The rts_l output can be set to an active low by programming bit 1 (RTS) of the Modem Control Register.
sin	Input	Serial input. Serial Data Input from the communications link (peripheral device, Modem or Data Set).
sout	Output	Serial Output. Composite serial data output to the communicatins link (peripheral, Modem or data set). The SOUT signal is set to the Marking Logic 1 state upon a Master Reset Operation.
xin	Input	External Crystal Input.
csout	Output	Chip Select Out. When asserted, indicates the core has been selected by assertion of the chip select inputs.
Txrdy_l	Output	In 16450 mode(FCR0 = 0),or FIFO mode0(FCR0=1 ,FCR3=0), and there are no characters in Tx FIFO, this pin is low active. It sets high after the first character is loaded into theXMIT FIFO or holding register. In FIFO mode1 this pin will be low active when there are no characters in Tx FIFO.This pin will become inactive when XMIT FIFO is completely full.
Rxrdy_l	Output	When in 16450 mode(FCR0=0, or in FIFO mode0(FCR0=1,FCR3=0), if there is at least one character in the Rx FIFO or Rx holding register,the RXRDY pin will be low active.It goes inactive when there are no more characters in the FIFO or holding register. In Mode1(FCR0=1,FCR3=1),when triger level or timeout interrupt has been reached,the rxrdy_l pin will go low active.Once activated,it will go inactive when there are no more characters in the FIFO.

Verification Models

The 16550 compatible UART has been extensively tested using the testbench developed at Comit Systems. The test bench is also available with the core.

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