Comit Systems, Inc.

PCI-X to PCI-X Bridge

Product Description 1.0

Features

- Complies with PCI Local Bus Specification rev 2.2, PCI-to-PCI Bridge Architecture Specification rev 2.0 and PCI-X Addendum to the PCI Local Bus specification rev 1.0a
- Supports configurations of PCI-X mode on either bus
- Primary and secondary interface clocks may be run synchronously or asynchronously
- Concurrent primary and secondary bus operations
- Standard PCI and device specific configuration registers, accessible from the primary interface
- Supports Type 0 and Type 1 configuration cycles
- 2KB of buffering for memory burst read commands, with up to four active transactions allowed
- 512 bytes of buffering for posted memory write commands, with up to four active transactions allowed
- Allows one active single data phase (4-byte) split transaction in each direction
- Supports full 64-bit addressing and Dual Address Cycles
- Programmable bus arbiter for the secondary bus with support for up to four external masters
- Priority and masking control for each agent
- Fully synthesized Verilog RTL source code.
- Fully functional Verilog test-bench
- Full synthesis support with synthesis scripts and constraint files for Synplicity and Design Compiler

PCI-X Bridge Core Facts	
Implementation details	
CLBs Used	**60%**
IOBs Used	**56%**
Device Type	**XCV1000 BG575 - 6**
Operating Frequency	**100 MHz**
Provided with Core	
Documentation	**Core Documentation**
Design File Formats	**Verilog Source code Synthesis Scripts**
Verification Tool	**Verilog-XL**
Test Bench	**Verilog Test Bench**
Design Tool Requirements	
Xilinx Core Tools	**M1 4.1i**
Entry/Verification Tools	**Verilog XL**
Synthesis Tools	**Synplify Pro v 7.0**
Support	
Support provided by Comit Systems, Inc.	

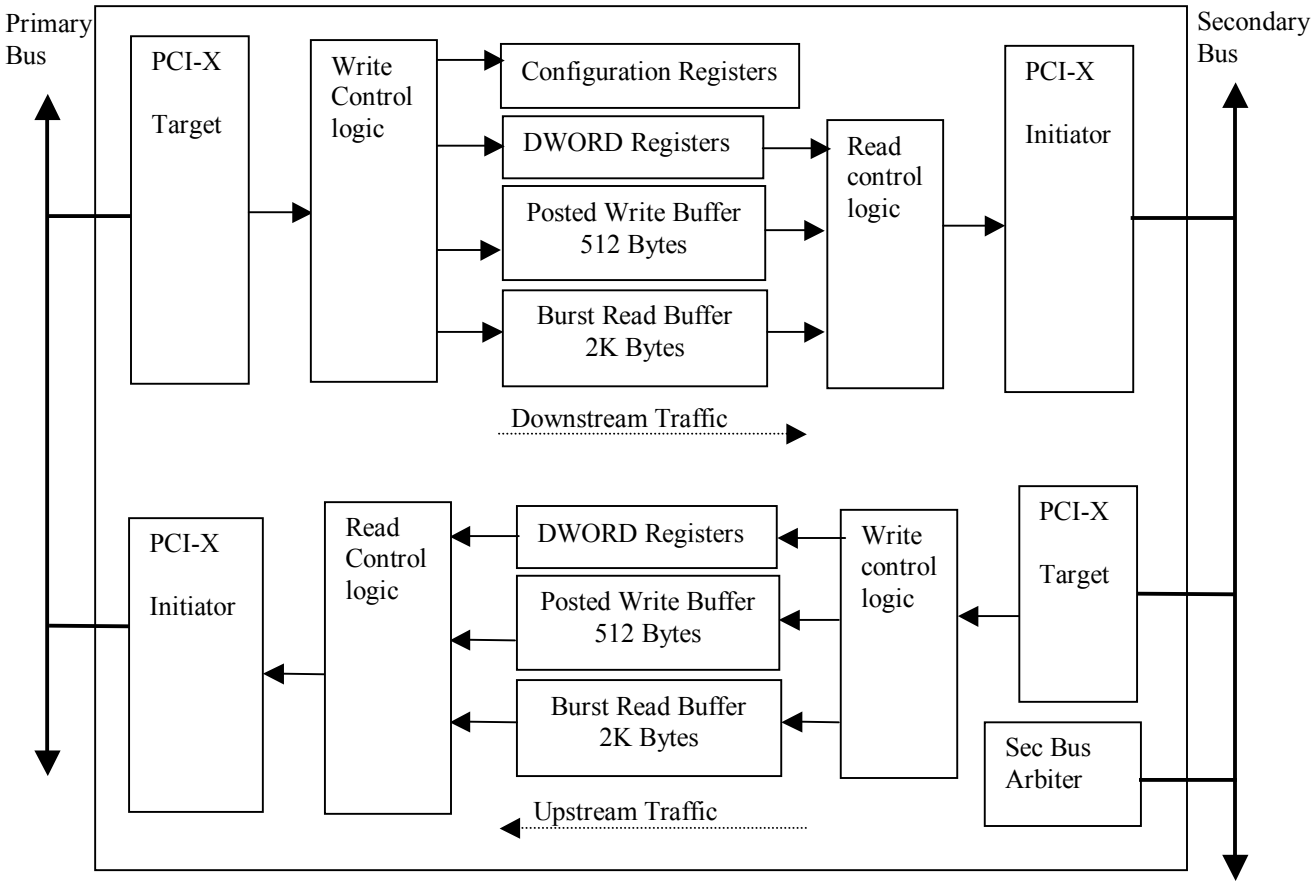

Fig 1 Block diagram of PCI-X to PCI-X Bridge

General Description

The PCI-X Bridge connects two electrically separate PCI-X bus domains. The bridge allows concurrent operations on both buses. This results in good utilization of the buses in various system configurations and enables hierarchical expansion of I/O bus structures.

The bridge has two control and data units, one for downstream transactions and one for upstream transactions. These symmetric units each contain separate buffers for burst read, posted write, and single data phase operations. Read and write queues, queue compare logic, address decoding, control logic, and other control functions are also included in these blocks.

An arbiter for the secondary bus, which can be disabled if an external arbiter is employed. When enabled, bus arbitration is provided for the bridge and up to four other masters. Each client can be assigned high or low priority, or can be masked off.

Functional Description

Supported Modes

The PCI-X bridge is a full-function transparent PCI-X to PCI-X bridge. Both interfaces supports the PCI-X bus protocol only. Each interface can be operated at maximum frequency of 100 MHz. Since the two clock domains are asynchronous and independent, a different bus speed may be used on each interface. The PCI-X Bridge implements a 64-bit bus on both interfaces. The PCI architecture also allows either side to be connected to a 32-bit bus or to 32-bit devices. Full 64-bit addressing capability is also provided, including support for dual address cycles (DAC).

Bridge Buffers

The PCI-X Bridge contains two symmetric sets of buffers with associated logic, one for upstream transactions and the other for downstream transactions.

A 512 byte memory is used as posted write buffer. This buffer is logically divided into four independent 128-byte segments. A single transaction can utilize from one to four 128-byte segments as needed.

A 2 KB memory is used as burst read buffer. This buffer is logically divided into eight independent 512-byte buffers. Each 512-byte buffer has a read queue providing up to four active read transactions in each direction.

A 4-byte buffer is used as data phase buffer for each direction to hold read or write data from split transactions. These transactions include all I/O or configuration operations as well as double word memory read operations.

Address Decoding

The PCI-X Bridge uses a flat addressing model. PCI-X address space is split between the primary bus and the secondary bus. Address ranges residing on the secondary bus are defined by the I/O, memory, prefetchable memory base and limit, and the optional base address registers 0 and 1 in the bridge configuration space. All other addresses are assumed to reside on the primary bus. Inverse address decoding is used to determine when to forward transactions upstream.

The PCI-X Bridge supports full 64-bit addressing and handles dual address cycles on both interfaces. The device provides no capability for translating addresses. The bridge configuration registers are accessible from the primary interface through Type 0 configuration reads and writes. On the secondary interface, the bridge claims Type 1 configuration write transactions that specify conversion to a special cycle on an upstream bus segment.

Bus Arbitration

The PCI-X Bridge contains an arbiter for the secondary interface that is enabled or disabled via an input signal pin. It provides bus arbitration for up to four additional masters, each of which may be assigned high or low priority or may be masked off. When the internal arbiter is being used and the PCI-X Bridge request is not masked off, the bus will be parked at the bridge whenever there are no pending requests.
The arbiter implements a two-level fairness algorithm that allows each device within a level to receive grant requests cyclically. The arbiter uses the arbitration priority register to determine which agents are high priority (HP) devices and which are low priority (LP) devices. At different points in time, snapshots are taken of all pending requests for each priority level. All captured HP requests are serviced first, then one of the captured LP requests is serviced. At this point, a new HP snapshot is taken, picking up any new HP requests. All captured HP requests are serviced before continuing with the next LP request still pending from the previous LP snapshot. A new snapshot of pending LP requests is taken only after all requests from the previous LP snapshot have been serviced.

Ordering Information
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