PCI-SDRAM CONTROLLER CORE

Product Description 1.0

Features

- Single chip PCI-SDRAM controller in a Xilinx XC4000XL FPGA to access 32MB of SDRAM
- Uses Xilinx LogiCORE PCI32 Version 2.0. Not included in deliverables.
- Operates up to 33.33MHz.
- Supports 64Mbit SDRAM
  - NEC uPD4564841-10
  - Toshiba TC59S6408BFTL-10
  - Micron MT48LC8M8A1/A2-10
- Uses auto refresh mode using internally generated refresh.
- Supports any length of burst cycles.
- Minimum bandwidth on Burst of 8 is 568 Mbps for Read and 710 Mbps for Write. Sample Cycles for burst of 8 requires 11 cycles for write and 15 cycles on read.
- Available in Verilog with extensive verification suites for functional, post-synthesis and post-layout verification.
- Can be customized by Comit Systems, or the customer, for following parameters:
  - SDRAM physical device type
  - SDRAM array width
  - Number of SDRAM banks
  - Various SDRAM speed grades
  - Other user application to go along with it.

AllianceCORE Facts
PCI-SDRAM Controller

Core Specifics	
	XC4013XLPQ240-1
CLBs Used	308/576
IOBs Used	224/1248
Operating Frequency	33.33MHZ
Device Features used	3-state buses
Supported Devices	
4013XL PQ208 -1	4013XLPQ240 -1
4028XLHQ240 -09	4028XLHQ240 -1
4062XLBG432 -09	4062XLBG432 -1
Provided with Core	
Documentation	Core User Guide XC4000E Datasheets
Design File Formats	Verilog Source code
Verification Tool	Verilog XL 2.05
Schematic Symbols	None
Constraint Files	User Constraints file
Evaluation Model	None
Reference Designs & Application notes	None
Design Tool Requirements	
Xilinx Core Tools	M1.5i
Entry/Verification Tools	Verilog XL 2.05
Synthesis Tools	Synopsys FPGA Express
Support	
Support provided by Comit Systems, Inc.	

Potential Applications

- Embedded applications in Telecommunication Systems
- High speed, high performance peripheral applications like printers
- DSP, image processing applications

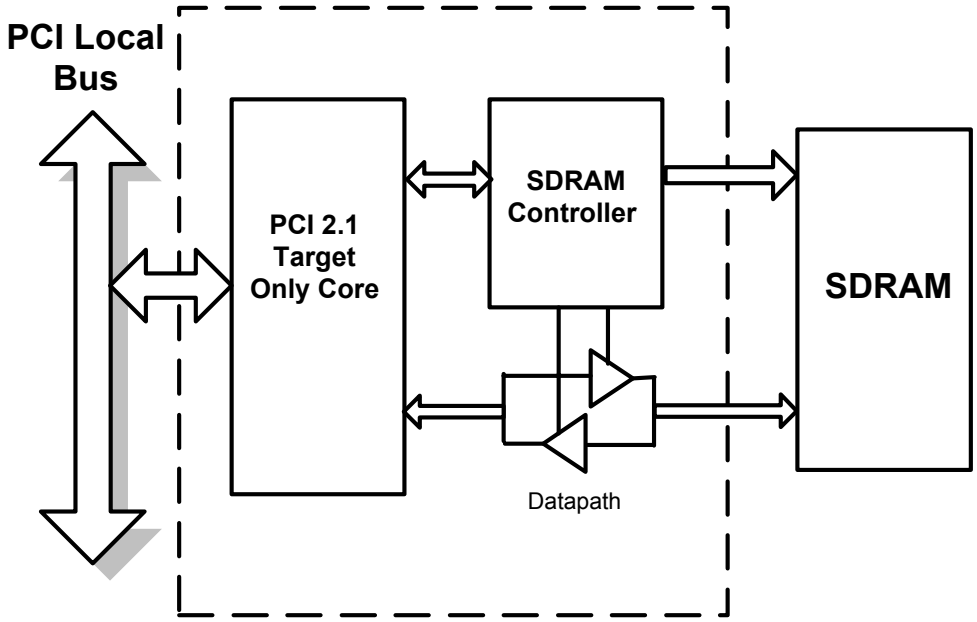

Figure 1. PCI-SDRAM Controller system Block Diagram

Recommended Design Experience

Knowledge of PCI specification is required. Knowledge of SDRAM desired. The user must be familiar with HDL design methodology in a hierarchical design environment.

General Description

PCI-SDRAM controller will be used for interfacing Xilinx Target Only PCI LogiCORE Version 2.0 with 32 Mbyte SDRAM. PCI-SDRAM controller takes decoded signals from PCI core and generates required sequence of operations for SDRAM. Controller is designed in such a way that it can be used with NEC uPD4564841-10, Toshiba TC59S6408BFTL-10 or Micron T48LC8M8A1/A2-10 which are 10ns parts with 2Meg X 8bits X 4 banks. The frequency of operation is 33MHz.

Functional Description

The PCI-SDRAM controller core is partitioned modules as shown in Figure 2 and described below.

PCI 2.1 Target only Core

This core is obtained from Xilinx and user needs to license it from Xilinx. This module interfaces with PCI local bus. It decodes cycles on the bus and presents it to SDRAM Controller. It presents datapath and control signals to and from SDRAM controller.

Address Latch and Incrementer

This module latches the address available from PCI core on internal bi-directional PCI address/data bus based on assertion of control signals. Row, column and bank addresses are generated from this address using following translation scheme.

PCI Address bit

24:13	: row address
12:11	: BA1:BA0
10:2	: Column address
1:0	: Ignored

Address Incrementer provides successive addresses for multiple write and read operations.

Finite State Machine

This state machine drives SDRAM Controller. The state machine, along with the input clock frequency, controls the timing of the SDRAM signals.

Auto Refresh generator

Refresh is done using CBR (auto-refresh). SDRAM Controller does refresh once every 15.625us. In design a counter provides a tick every 15us. This request will not interrupt the ongoing cycle immediately. It will allow 16 read or write operations to happen (16 clock cycles) and then generate interrupt which will terminate ongoing cycle.

KEEPOUT	Out	Keepout

Core Modifications

The PCI-SDRAM controller core design is modular; making modifications is relatively simple. If you are interested in obtaining a version of the core that is different from this product description, then contact Comit Systems directly. Comit Systems can provide custom version of core, including the changes in SDRAM interface, changes in memory type, configurations and adding the additional other application specific features required.

Pinout

The pinout of the PCI-SDRAM controller is shown in the Table 1 below.

Signals used by SDRAM Controller on PCI side

Symbol	Type	Name
ADIO[31:0]	I/O	Address/Data Bus
PCI_CMD	In	PCI Bus Command
ADDR_VLD	In	Address valid
BASE_HIT[7:0]	In	Base Address Hit
S_DATA_VLD	In	Slave Data valid
S_WRDN	In	Slave Write / Read Direction
S_SRC_EN	In	Slave data Source Enable
S_READY	Out	Slave Ready
S_TERM	Out	Slave Terminate Transaction
T_ABORT	Out	Target Abort
S_CBE[3:0]	In	Slave Command / Byte Enables
PCI_RST	In	PCI Reset
PCLK	In	Input Clock
CLK	Out	PCI Clock
C_READY	Out	Configuration Ready
C_TERM	Out	Configuration Terminate transaction
INTR_N	Out	Interrupt
SUB_DATA [31:0]	Out	Subsystem / Subsystem Vendor ID

SDRAM side pins

Symbol	Type	Name
CLK	Out	Master Clock
A[11:0]	Out	Address Bus
CS_n	Out	Chip Select
RAS_n	Out	Row Address strobe
CAS_n		Column Address Strobe
WE_n		Write Enable Strobe
DQM[3:0]	Out	Data Input/Output Mask
BA1 BA0	Out	Bank Address
CKE	Out	Clock Enable

Verification methods

The PCI-SDRAM controller has been tested extensively using the testbench developed at Comit Systems. The testbench is also available with the core.

Comit Systems, Inc.
3375 Scott Blvd. Ste 139
Santa Clara, CA 95054, USA.
Phone: +1 (408) 988-2988

URL: http://www.comit.com

FOR MORE INFORMATION CLICK THE REQUEST QUOTE LINK ON WEBSITE