Single Channel HDLC Controller

Product Description 1.0

Features

- Fully Compliant to ISO 3309 specifications
- HDLC ISO / OSI Layer 2 functions including:
  - ♦ Flag, Idle and Abort Generation / Detection
  - ♦ Zero Deletion / Insertion
- Operates up to 4 Mbps
- Serial Line Interface
- NRZ / NRZI Encoding and Decoding
- Supports Modem Control Signals (RTS, CTS and CD)
- CRC-16 / CRC-32 Generation and Checking
- CRC Disable Control
- Interface for Two External FIFOs (64 x 9 bit)
- Terminal Data Loop Back Facility
- Transparent Mode
- Supports Shared Opening and Closing flags between Frames
- Supports Idle and Flags in Interframe-time-fill
- Includes following Error Detection capabilities:
  - ♦ Abort / CRC Error
  - ♦ Non-octet frame Content

AllianceCORE Facts
Single Channel HDLC Controller

Core Specifics		
	XC4000E	
CLBs Used	214	
IOBs Used	50	
Serial Clock	4MHZ	
Device Features used	3-state buses	
Supported Devices		
	I/O	CLBs
XC4006E-3 PC84	50	214
Provided with Core		
Documentation	Core Documentation XC4000E Datasheets	
Design File Formats	VHDL Source code	
Verification Tool	ModelTech V-System Tools	
Schematic Symbols	None	
Constraint Files	Time Spec. Files	
Evaluation Model	None	
Reference Designs & Application notes	None	
Design Tool Requirements		
Xilinx Core Tools	XACT step	
Entry/Verification Tools	ModelTech V-System Tools	
Synthesis Tools	Synopsys Design Compiler	
Support		
Support provided by Comit Systems, Inc.		

Potential Applications

- Embedded applications in Telecommunication Systems
- Applications in X.25, LAPB and ISDN LAPD Communication Systems
- Applications in point to point Communication Links

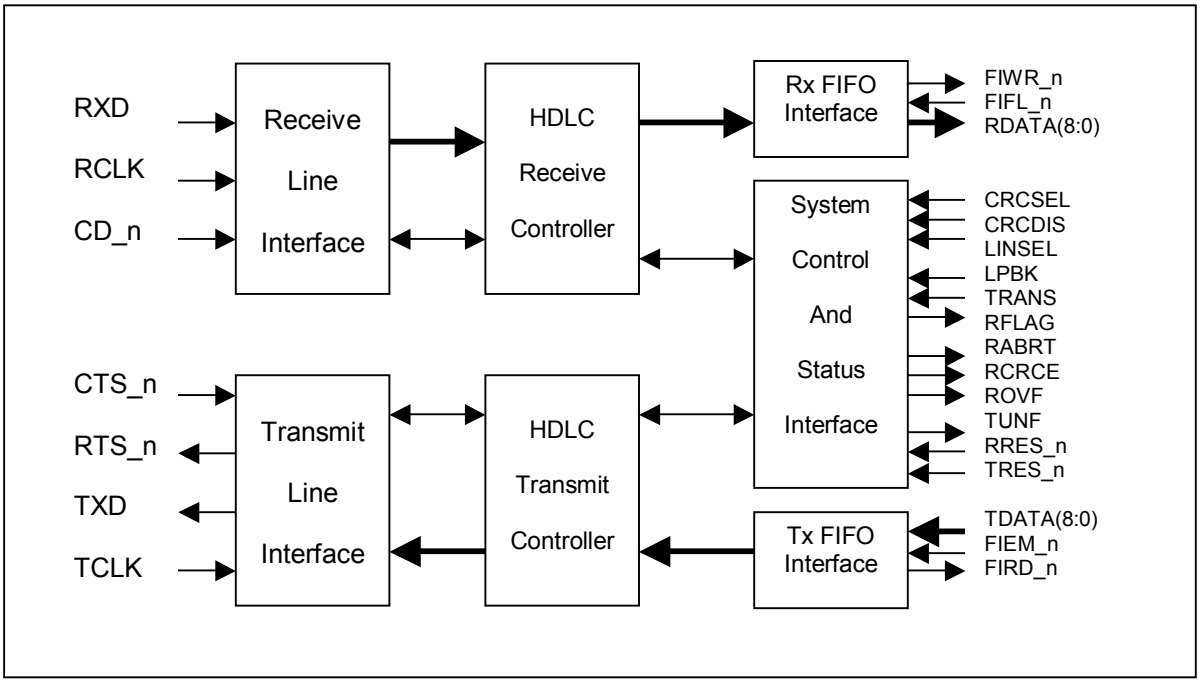

Figure 1. Single Channel HDLC Controller Block Diagram

Recommended Design Experience

Knowledge of HDLC specification is required. The user must be familiar with HDL design methodology in a hierarchical design environment.

General Description

The HDLC Controller is flexible and the interfaces can be customized for any microcontroller based applications. The core includes the functionality for a complete HDLC controller.

Functional Description

The HDLC controller core is partitioned into seven modules as shown in Figure 1 and described below.

Receive Line Interface

The Receive Line Interface handles NRZI decoding and active clock selection for HDLC receive operation.

HDLC Receive Controller

The HDLC Receive Controller handles Flag detection, Abort detection, Idle detection, Zero deletion, CRC Checking and Serial to parallel conversion of receive data.

RxFIFO Interface

The RxFIFO Interface handles the write FIFO accesses, end of frame detection and FIFO overflow error.

System Status and Control Interface

The System Status and Control Interface consists of General control interface, Receive control interface and Transmit control interface. The General control interface handles CRC polynomial selection, CRC enable control, Line encoding scheme selection, Loopback mode control and transparent mode control. The Receive control interface handles receive clock selection, receive reset and receive status/error indications. The transmit control interface handles transmit clock selection, transmit reset and transmit status/error indications.

TxFIFO Interface

The TxFIFO Interface handles the read FIFO accesses and FIFO underflow error.

HDLC Transmit Controller

The HDLC Transmit Controller handles parallel to serial conversion, CRC generation, Zero insertion (bit stuffing), abort generation and flag insertion.

Transmit Line Interface

The Transmit Line Interface handles NRZI encoding and active clock selection for HDLC transmit operation.

Core Modifications

The single channel HDLC controller core design is modular, making modifications is relatively simple. If you are interested in obtaining a version of the core that is different from this product description, then contact Comit Systems directly. Comit Systems can provide custom version of core, including the changes in microprocessor interface, changes in line interface and adding the additional features required.

Pinout

The pinoout of the HDLC controller has not been fixed to specific FPGA I/O allowing flexibility with user application. The signal names are provided in the Table 1 below.

Signal	Signal Direction	Package Pin	Description
Line Interface Signals			
RXD	Input	I/O	Receive Serial Data
RCLK	Input	I/O	Receive clock
CD_n	Input	I/O	Carrier Detect
TXD	Output	I/O	Transmit serial Data
TCLK	Input	I/O	Transmit Clock
RTS_n	Output	I/O	Request to Send
CTS_n	Input	I/O	Clear to Send
FIFO Interface Signals			
FIWR_n	Output	I/O	FIFO Write
FIFL_n	Input	I/O	FIFO Full
RDATA[8:0]	Output	I/O	Receive Data
FIRD_n	Output	I/O	FIFO Read
FIEM_n	Input	I/O	FIFO Empty
TDATA[8:0]	Input	I/O	Transmit Data
System Control and Status Signals			
CRCSEL	Input	I/O	CRC Select
CRCDIS	Input	I/O	CRC Disable
LINSEL	Input	I/O	Line Code Selection
LPBK	Input	I/O	Loop back
TRANS	Input	I/O	Transparent mode
RRES_n	Input	I/O	Receive Reset
RCINV_n	Input	I/O	Receive Clock invert
RXF_n	Output	I/O	Receiving Frames
RFLAG	Output	I/O	Receive Flag
RABRT	Output	I/O	Receive Abort
RIDLE	Output	I/O	Receive Idle
RCRCE	Output	I/O	Receive CRC Error
ROVF	Output	I/O	Receive overflow
CDLE	Output	I/O	Carrier Detect Lost Error
TRES_n	Input	I/O	Transmit Reset
TCINV_n	Input	I/O	Transmit Clock Invert
TXF_n	Output	I/O	Transmitting Frames
TFLAG	Output	I/O	Transmit Flag Indication
TABRT	Output	I/O	Transmit Abort Indication
TUNF	Output	I/O	Transmit Underflow
CTSLE	Output	I/O	Clear To Send Lost Error
CTSLE	Output	I/O	Clear To Send Lost Error

Verification methods

The single channel HDLC controller has been tested extensively using the testbench developed at Comit Systems. The testbench is also available with the core.

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