Comit Systems, Inc.

1024 Point FFT Core

Product Description 1.0

Features

- High-performance 1024-point, radix-4 complex FFT
- 16-bit complex input and output data
- 2's complement arithmetic
- Uses Virtex-II on-chip Block RAM, no external memories needed
- Naturally ordered input and output data
- Extensive Test bench and test case available
- Full synthesis support with synthesis scripts and constraint files for Synplicity
- Can be customized by Comit Systems, or the customer for any user applications

Potential Applications

- Applications in Telecommunication Systems
- DSP and image processing applications

IP CORE Facts 1024 Point FFT	
Core Specifics	
Device	XC2V250-FG256-4
CLB s Used	140/384
SLICEs Used	925/1536
IOBs Used	70/172
Operating Frequency	70 MHZ
Transform Time	6200 clock cycles (approx.)
Device Features used	Block RAMs, 18x18 signed multiplier.
Supported Devices	
XC2V250-FG256-4, 5, 6	
Provided with Core	
Documentation	Core User Guide XC2V250 Datasheets
Design File Formats	VHDL Source code
Constraint Files	User Constraints file
Design Tool Requirements	
Xilinx Core Tools	Design Manager 3.3
Entry/Verification Tools	ModelTech MTI 5.5a
Synthesis Tools	Synplicity's Synplify 6.2.4
Support	
Support provided by Comit Systems, Inc.	

OVER…

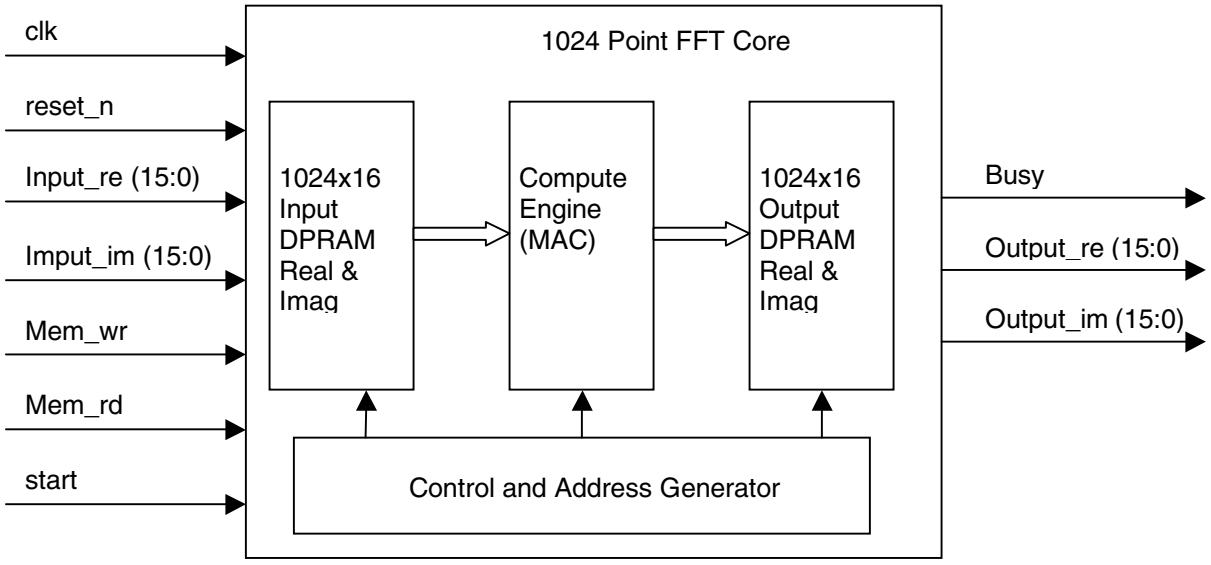

Figure 1. FFT Core Block Diagram

Recommended Design Experience

Knowledge of DSP and FFT is required. The user must be familiar with HDL design methodology in a hierarchical design environment.

General Description

The FFT Core computes a 1024-point complex forward FFT. The input data is a vector of 1024 complex values represented as 16-bit 2's complement numbers – 16-bits each, for the real and imaginary components of a data sample.
The 1024 element complex output vector is also represented using 16 bits for each of the real and imaginary components of an output sample.

Functional Description

The FFT core is partitioned into three major modules namely Memory section, Multiply and Accumulate, and Control and Address Generator.

Memory Section

The core has three memory areas – two 1024 x 16 DPRAMs for storing the input samples, two 1024 x 16 DPRAMs for storing the output results and two 768 x 16 ROMs for storing the Twiddle Factors.

Multiply and Accumulate Section

This is the heart of the FFT core as FFT basically involves multiplication and adding. It also includes the pipelines needed for the data to be properly present at the Multiplier and adder inputs.

Control and Address Generator

This block is the main controller block. It contains the SM for keeping track of computation stages, and generates addresses and R/W control signals to all memories as needed. It also handles the interface signals such as memory write/read and the Start/Busy signals.

Verification methods

The FFT core has been tested extensively using the testbench developed at Comit Systems. The testbench is also available with the core. Various input patterns are input to the core. The same patterns are also given to a standard FFT implementation using MATLAB. The outputs from the core are compared to the outputs obtained from MATLAB.

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