COMIT SYSTEMS
The Contract Engineering Company

Ethernet – RF Bridge Controller

(Customize for bridging to UWB, 802.11x, etc.)

Product Description 1.0

Features

- MAC layer bridging between 10/100 Mbps Ethernet and RF Protocols (UWB, 802.11, HomeRF or HiperLAN)
- Efficient architecture; Independent bus for data transfer
- Flexible Queue Manager in hardware, minimizing software overhead
- On-Chip buffer of 32K bytes; Can be increased to 64K or 128K bytes
- 32 bit wide DPRAMs are used to store buffer descriptors and packet headers
- Timers, Interrupt Controller and UART are available
- ARM CPU based design
- ASB bus connects all the peripherals to the ARM CPU
- Uses third party 10/100 Ethernet core
- Design Prototyped in Xilinx XCV2000E device; Test chip used for ARM CPU

Ethernet – RF Bridge Controller	
Core Specifics	
	XCV2000E
CLBs Used	7250
IOBs Used	242
Block RAM Used	83
Provided with Core	
Documentation	Core Specification
Design Format	Verilog Source code
Testbench Format	Verilog testbench
Constraint Files	Synplify and DC constraints
Design Tool Requirements	
Xilinx Core Tools	Alliance Elite
Verification Tool	NC-Verilog
Synthesis Tools	Synplify / Synopsys DC
Support	
Support provided by Comit Systems, Inc.	

Potential Applications

1. RF Bridge for Networking using UWB, 802.11, HiperLAN and HomeRF protocols
2. Development platform for Ethernet bridges

General Description

The block diagram of the Ethernet-RF Bridge Controller is shown in Figure 1. The Bridge Controller provides capabilities to build IEEE802.1D compliant transparent bridge between Ethernet MAC and RF MAC.

Functional Description

Queue Manager

Queue Manager maintains a linked list of buffers in six queues. Three queues each are used in Ethernet and RF MAC. The design requires software to create the buffers and add them to the Free Queues on each side during system initialization. Any number of buffers with any size can be created based on available memory in the system and based on the type of traffic expected.

When a packet is received, a buffer is taken out of the Free Queue to store the packet and added to the Receive Queue by the hardware. Software can de-queue the packet from Receive Queue and process it. If Software decides to drop the packet, the buffer is added to Free Queue. If Software decides to forward the packet on to the RF side, it translates the header and adds the packet to Transmit Queue of the RF section. Software can reorder the buffers in the queue. Once the packet is successfully transmitted, the buffer is added back to Free Queue by hardware.

Ethernet section

Third party 10/100 Mbps Ethernet Core is integrated in the design. Ethernet control logic moves the header of each packet to Header DPRAM and moves the whole packet to the Shared Data Buffer. CPU has a dedicated port for accessing the header in the Header DPRAM. Queue manager and Ethernet control logic shares the other port of DPRAM. Status of each packet received is stored in the descriptor section of the buffer.

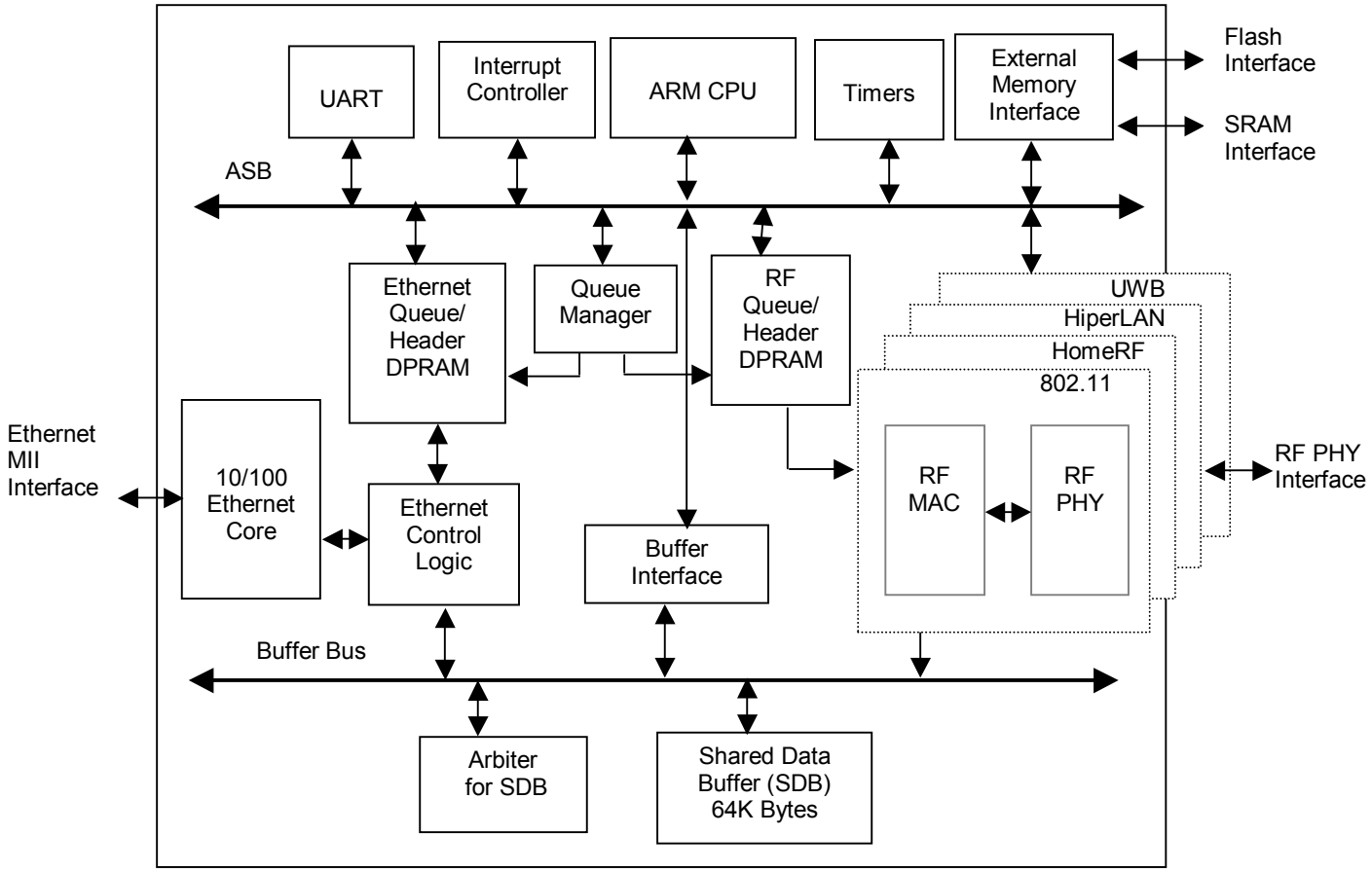

Figure 1. Block diagram of Ethernet-RF Bridge Controller

RF Section
The RF MAC and the digital section of the RF PHY can be integrated. Comit has expertise in designing RSA's RC4 based Encryption/Decryption modules and Forward Error Correction (FEC) modules. Other available crypto core designs include DES / TDEA (FIPS-46-3) and AES (FIPS-197).

Shared Data Buffer
A single port SSRAM is used as the Shared Data buffer between the Ethernet and RF sections. The CPU can also access this buffer through the Data Buffer Interface Module. An arbiter is used to manage the ownership of the bus. All the agents access the memory using burst transfers.

External Memory Interface
External Memory Interface supports Flash and SRAM interfaces. 32-bit wide SRAM can be used at this interface.

Ordering Information
Enquiries for this product may be directed to:

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