Comit Systems, Inc.

Viterbi Encoder/Decoder

Features

- **Maximum Data throughput 100Mbps**
- Parameterized Constraint length from K = 3 to 13
- Parameterized Code rates =1/2 or 1/3
- 1bit hard decision or Parameterized soft decision length decoding
- Hamming distance as Branch Metric (BM) in case of hard decision and Euclidean Metric as BM in case of soft decision
- Serial or parallel Interface for the decoder/encoders (synchronization unit in case of serial Interface)
- Parameterized polynomials G0, G1, and G2 (in case of code rate=1/3) for decoder
- Parameterized polynomials G0, G1 and G2 for encoder
- Parameterized decision depth L
- Maximum Operating Frequency 100MHz
- Fully Parallel Architecture
- Registered I/O and fully synchronous design with single clock
- Fully synthesized Verilog® RTL source code
- Fully functional Verilog and TCL testbench
- Full synthesis support with synthesis scripts and constraint files for Synplicity®
- Scripts for Placement and Routing for Xilinx® series are also available. Generates SDF back-annotated Verilog files for post layout simulation
- Memory is embedded inside the core, can be easily changed to external memory

Viterbi Decoder Core Facts	
Memory Usage	
DPRAM	Depends upon K and L parameters It is 4 blocks of 2^{K-1} * (L + tbstart_latency) bits minimum
Core Constraints	
Initial latency	4 * L + 3 * tbstart_latency + 6
Implementation details (for K=7,code rate=1/2, L=35, device XC2V3000-6-bf957, decoder only with parallel input interface)	
SLICESs Used	3735 out of 14336 (26%)
IOBs Used	9 out of 684 (1%)
No. of BLOCKRAMs	8 out of 96 (8%)
Operating Frequency	100Mhz
Number of BUFGMUXs	1 out of 16 (6%)
Initial Latency	155 clocks
Tbstart_latency	3
Provided with Core	
Documentation	Core Documentation
Design File Formats	Verilog Source code Synthesis Scripts
Test Bench	TCL Test Vectors
Evaluation Model	TCL based model
Reference Design & Application Notes	Viterbi Tutorial
Design Tool Requirements	
Xilinx Core Tools	ISE 4.2i Foundation
Entry/Verification Tools	NC-Verilog and TCL
Synthesis Tools	Synplify ver 7.0
Support	
Support provided by Comit Systems, Inc.	

Potential Applications

- Embedded applications in Telecommunication Systems
- Data Storage and Communication Systems
- Applications in point to point and point to multi-point Communication Links

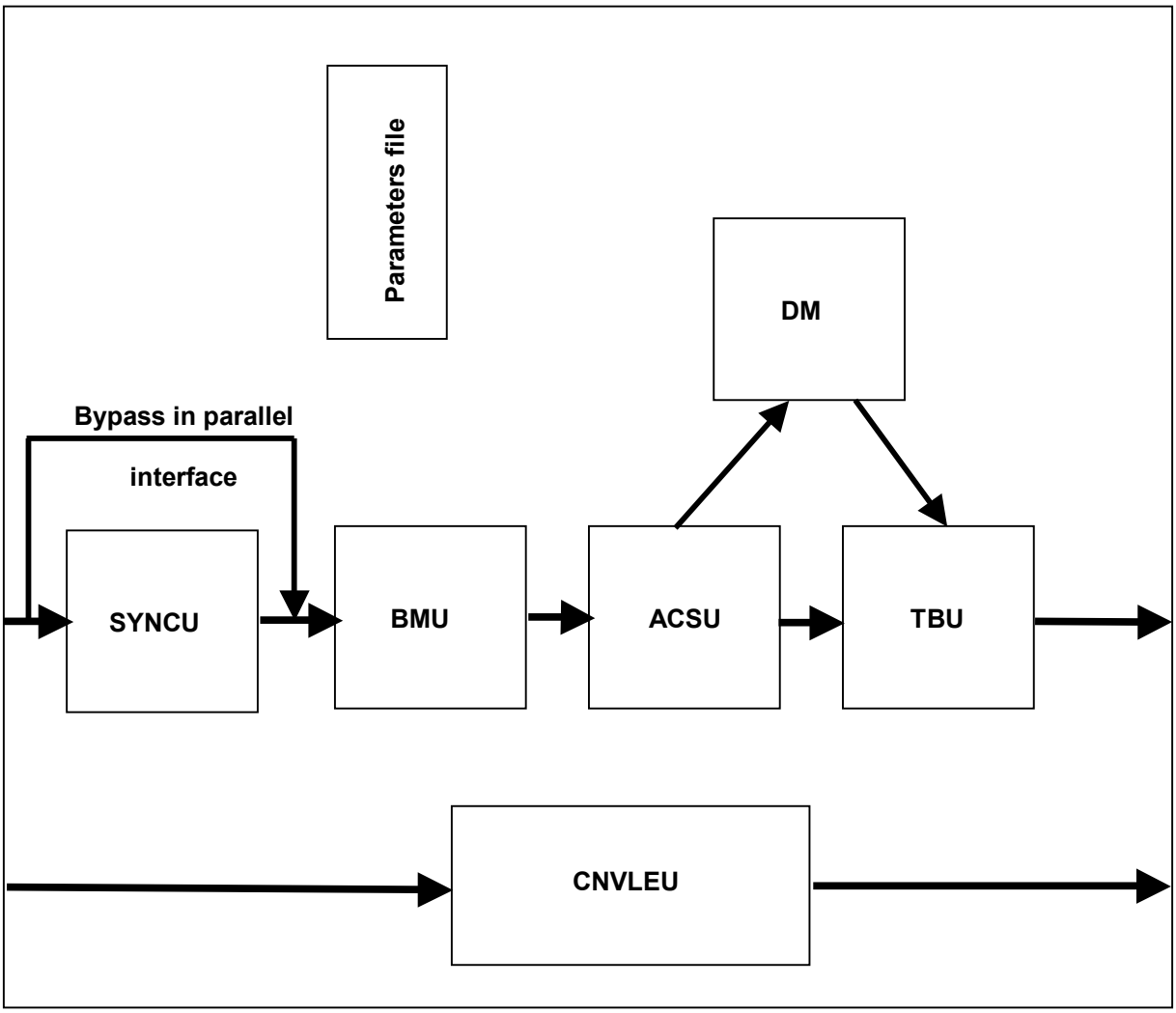

Figure 1. Viterbi Encoder/Decoder Block Diagram

General Description

Convolutional Encoding and Viterbi Decoding are used to provide forward error correction, which improves digital communication performance over a noisy channel. Viterbi Algorithm realizes the maximum-likelihood decoding of Convolutional codes received in applications such as terrestrial, satellites, digital modems, digital cellular telephone applications, WLAN and others.

Functional Description

The Viterbi Decoder core is partitioned into several sub blocks as shown in Figure 1. Its main function is to decode convolutionally encoded data transmitted over the channel with correction of erroneous data bits and is ideal for the Gaussian type of channel.

Synchronization Unit (SYNCU)

This is the synchronization unit of the design, which synchronizes the decoder at the symbol boundary by monitoring the Path Metric (PM) normalizations.

The decoder is designed to iteratively sync symbol boundary with the encoder by shifting its symbol boundary by one bit at a time if PM normalization happens too often. The “too often” number is software configurable.

The worst-case scenario will take *n* (code rate=1/n) such iterations before coming into sync. The status of decoder is reported to the system via the STATUS port.

Branch Metric Unit (BMU)

This unit computes the Branch Metric (BM) for the received symbol. In case of hard decision, BM is taken as the Hamming distance between received symbol and the encoder output corresponding to a particular state transition. In case of soft decision, BM is taken as Euclidean distance.

Add Compare and Select Unit (ACSU)

The ACSU unit is used to compute the path metric at any node and decide on any one of the incoming paths converging at one node. The decoder implements adders for computing the path metric and a compare-select section to decide on the best path. The updated Path Metrics are written into the Path Metric Registers and decision bits in the Decision Memory (DM). In parallel architecture, there are *n* ACS units, where *n* is the number of states.

Trace Back Unit (TBU)

During the decoding process the decoding information is stored in the decision memory. This unit reads the decision data from this memory and decodes it. The trace back length is parameterized. Determining the minimum path metric out of *n* (2 to power K-1) Path Metrics is critical for design performance. This core's architecture is designed to improve the performance by increasing the Decision memory by X locations, where X is the number of clock cycles taken by the design in determining the minimum path metric.

Convolutional Encoder Unit (CNVLEU)

The encoder of a binary convolutional code with rate *1/n* may be viewed as a finite state machine that has a M-stage shift register with prescribed connection to *n* modulo-2 adders and a multiplexer, which serializes the outputs of the adders. Fig 2 shows the block diagram of code rate 1/2 encoder. The constraint length (K) is defined as the number of shifts over which a single message bit can influence the encoder output. In an encoder with 'M' stage shift register, constraint length K=M+1. Each path connecting the input to the output may be characterized by the impulse response, defined in terms of polynomials called generator polynomials. This is the generalized convolutional encoder for code rate = 1/2 or 1/3 with the parameterized generator polynomials G0, G1, and G2 (in case of code rate = 1/3).

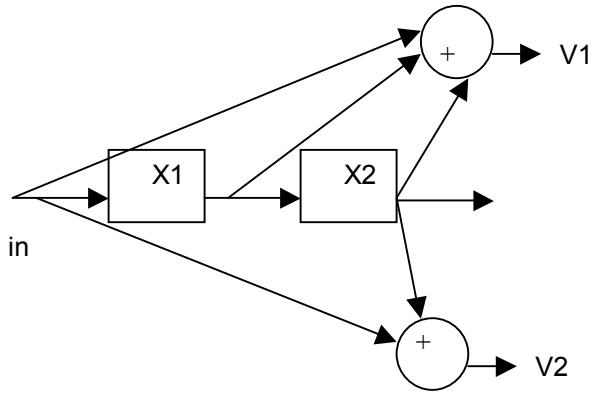

Figure 2. Code rate ½ encoder with G0 101 and G1 111

Verification methods

The Viterbi decoder core has been verified functionally using the test bench developed at Comit Systems. The test bench was developed using Verilog and TCL. The test vectors were written in TCL.

Pinout

The pinout of the Viterbi Decoder can be configured to any FPGA I/O. The signal names are provided in Table 1 below.

Table 1. Signal Names

Signal	*Direction*	*Size*
CLK	Input	
RESET_N	Input	
CLEAR	Input	
DEC_DATA_INV	Input	
DEC_DATA_IN	Input	[n:0]
DATA_OUT	Output	
DATA_OUT_V	Output	
ENC_DATA_IN	Input	
ENC_DATA_OUT	Output	[n:0]
NORM_CNT	Input	[`norm_cnt_width-1:0]
DECSTG_CNT	Input	[`dec_stg_cnt_width-1:0]
STATUS	Output	1 bit

Table 2. Parameter Descriptions

Parameter name	Description
Constraint (K)	Constraint length for the de-coder/Encoder
Coderate	0 => code rate 1/2 1 => code rate 1/3
Soft_hard_n	0 => hard decision 1 => soft decision
Decision depth (L)	Decision depth
Poly G0	G0 polynomial
Poly G1	G1 polynomial
Poly G2	G2 polynomial (in case of 1/3 code rate)
Soft_length	Soft decision length Should be 1 in case of hard decision.
Parallel	1 = parallel data in interface 0 = serial data in interface
Tbstart_lat	The number of clocks in deciding the Minimum Path Metric out of N path metrics. This parameter is dependent on targeted design speed and technology.

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