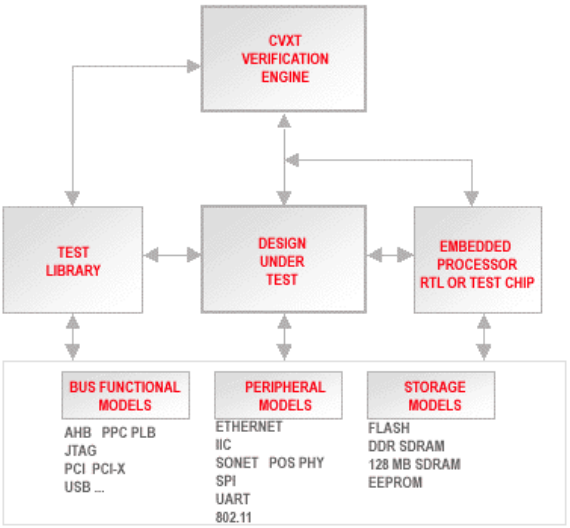
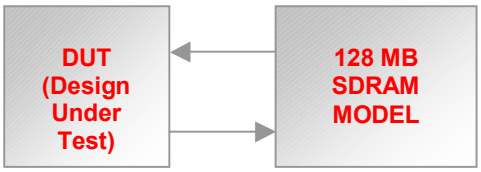
Fiesta® 128MB Synchronous DRAM Model

Features

- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Refresh Mode
- Self Refresh Mode
- 64ms, 4,096-cycle refresh (15.6µs/row)
- Supports CAS latency of 1, 2, and 3



System Interface Diagram



Fiesta® Process Standardization and Acceleration Tool Kit is an industrial strength suite of tools designed, developed, tested and used by engineers of Comit's Contract Engineering Center. Their experience in developing processes and methodology that yield predictable and accurate results forms the foundation of the toolkit. Use it with confidence.

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