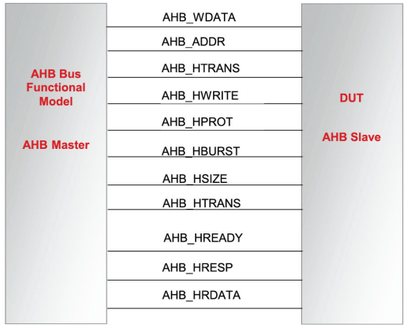
Fiesta® AHB Bus Functional Model

Features

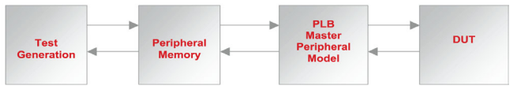
- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- Configurable to test different types of AHB slaves and all possible AHB burst sizes
- Internally generated clock signal with parameterized frequency
- Descriptors to set the following:
  - AHB burst type (SINGLE, INCR, INCR4, WRAP4, INCR8, WRAP8, INCR16, WRAP16).
  - Increment size in case of INCR burst.
  - Hsize (BYTE, HALFWORD, WORD).
  - Hprot (Cacheable, Bufferable, Privilege, Data/opcode)
  - Start Address for a burst.
  - Start data for Write access.
  - Busy cycle insertion within a burst.
  - Idle cycle insertion between bursts.
  - Burst terminate and Locked transfer
- 32 bit wide memory



Fiesta® PLB Master Peripheral Model

Features

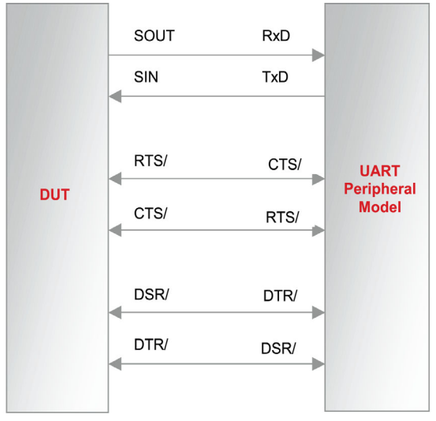
- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- Tests PLB Master/Slave & PLB Slave devices
- Sideband signals control model behavior to simulate different conditions
- Creates different accesses to the PLB Bus based on the contents of Peripheral Memory (See Comit Fiesta® CMMT Memory Model)
- PLB Access information provided by control DWORD
- Supports line, non-line, burst and non-burst transfers
- Master bus width settable from 32 bits to 256 bits
- Programmable Master Transfer Size and Master Transfer Type
- Implements 4 levels of Master Request Priority
- Supports
  - Master Compressed Data Transfer
  - Master Guarded Memory Access
  - Master Ordered Transfer



Fiesta® UART Peripheral Model

Features

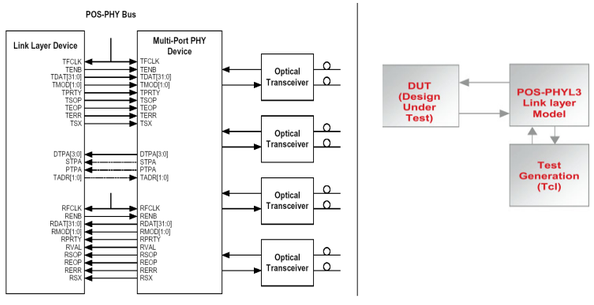
- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- Configurable to test different types of 16550 compatible UART systems
- Internally generated clock signal with parameterized frequency
- Descriptors to set the following:
  - Baud rate division factors (from 1 to 2^{16} –1 of clock).
  - Number of data bits (5 to 8)
  - Number of stop bits (1, 1.5, 2)
  - Parity (none, odd, even
  - Idle delay
- 32 bit wide memory



Fiesta® POS-PHYL3 Peripheral Model

Features

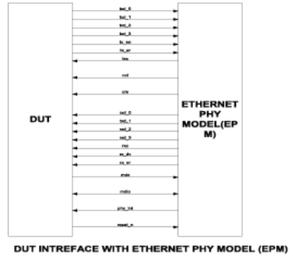
- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- Configures POS-PHY Layer 3 protocol for Link Layer Device
- Sideband signals control model behavior to simulate different conditions
- Number of ports: 1 to 48 links
- Data bits width: 8 or 32 bits
- Descriptors to set the following:
  - Packet mode or Byte mode
  - Packet size up to 512 bytes
  - Packet Buffer Size
  - Inter Packet Gap
  - Parity Error Control
  - Packet Flow Pausing



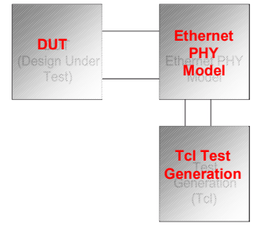
Fiesta® Ethernet PHY Model

Features

- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- Interfaces with Comit Fiesta® CMMT memories
- Tests DUT containing an Ethernet MAC core
- Based on MII interface
- Link model for Tx and Rx
- Provides the following test functionality:
  - Transmission by DUT
  - Reception by DUT
  - CRC Generation and checking
  - Forced Collisions
  - Forced Receive Errors



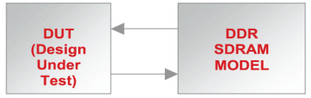
DUT INTREFACE WITH ETHERNET PHY MODEL (EPM)



Fiesta® DDR SDRAM Model

Features

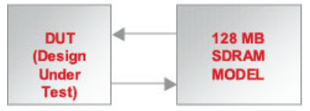
- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- Bidirectional data strobe (DQS) transmitted/ received with data, i.e., source-synchronous data capture (x16 has two – one per byte)
- Internal, pipelined double-data-rate (DDR) architecture; two data accesses per clock cycle
- Differential clock inputs (CK and CK#)
- Commands entered on each positive CK edge
- DQS edge-aligned with data for READs; center-aligned with data for WRITEs
- DLL to align DQ and DQS transitions with CK
- Four internal banks for concurrent operation
- Data mask (DM) for masking write data (x16 has two – one per byte)
- Programmable burst lengths: 2, 4, or 8
- Auto Refresh and Self Refresh Modes



Fiesta® 128MB Synchronous DRAM Model

Features

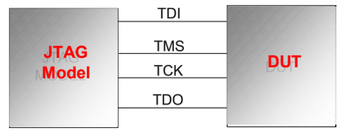
- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- PC100 functionality
- Fully synchronous; all signals registered on positive edge of system clock
- Internal pipelined operation; column address can be changed every clock cycle
- Internal banks for hiding row access/precharge
- Programmable burst lengths: 1, 2, 4, 8, or full page
- Auto Refresh Mode
- Self Refresh Mode
- 64ms, 4,096-cycle refresh (15.6µs/row)
- Supports CAS latency of 1, 2, and 3



Fiesta® JTAG Model

Features

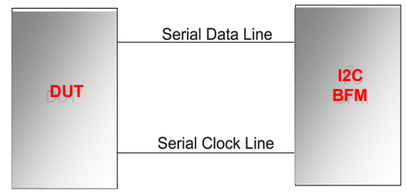
- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- Generates stimuli to test any device that has a JTAG boundary scan circuit
- Generates all standard JTAG commands
- Data scan in through TDI
- Data capture from TDO



Fiesta® I²C Bus Functional Model

Features

- Interfaces with Comit Fiesta® CVXT Open Verification Environment
- Master & Slave models available for testing slave & master devices
- Each device (I²C slave) can be assigned an address
- Bit rate settable to 100Kbits/sec, 400Kbits/sec or 3.4Mbits/sec



Specifications

Inputs

- DUT Verilog code
- BFMs, PMs and memory models: Verilog, C
- Tests: tcl
- Top level control: Tcl

Outputs

Test logs; Test results: .LOG, .RPT

Platforms

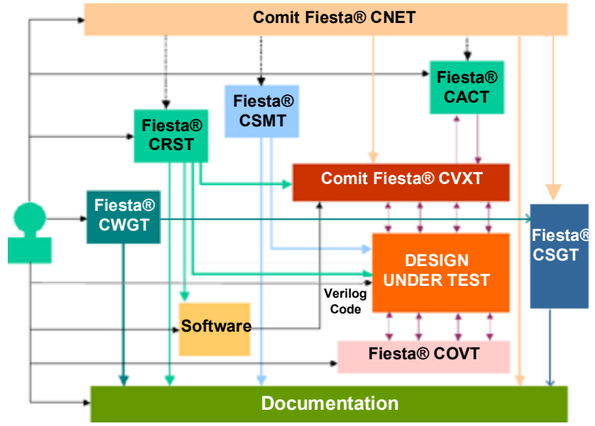
OS	Ver.	Simulator	Ver.
Solaris (Sparc)	2.7	nc-Verilog	3.2/3.3/3.4
Solaris (Sparc)	2.7	modelsim	5.6
Windows NT	4.0	nc-Verilog	3.4
Windows NT	4.0	modelsim	5.6

Comit Fiesta® CVXT is part of the Comit Fiesta® Process Standardization & Acceleration Toolkit. Individual tools are designed to work in standalone mode or in cascade, where the output of one tool can be used by another.

Fiesta® Process Standardization & Acceleration Toolkit is an integrated set of tools with a vision to painlessly transform specification to product, by producing as much of code and documentation automatically as possible, and simultaneously setting up a compatible verification environment from the start. Designers, therefore, are free to focus on designing state machines and creating tests. Coexists with industry standard EDA tools for simulation, synthesis and layout.

The toolkit consists of the following additional tools:

Fiesta® CRST Register Specification Tool
Accepts register bank definitions for a chip. Generates and regenerates documentation, software interface definitions, hardware implementations and verification definitions, preserving consistency, and avoiding errors



Fiesta® CSMT Finite State Machine Editor
Generates synthesizable Verilog code, and diagrams for documentation from state machines.

Fiesta® CMMT Simulation Memory Modeler
Generates dynamically configurable simulation time memory models that can be used in advanced system-level verification

Fiesta® CSGT Synthesis Script Generator
Accepts constrains and generates script to automate synthesis flow for popular synthesis tools

Fiesta® CAVT AHDL to VHDL Conversion tool
Converts Altera's proprietary HDL - AHDL to portable VHDL files to target any technology

Fiesta® CWGT Waveform Generation Tool
Produces output signal waveforms based on a GUI based input of signals and their transitions.

Fiesta® CACT Architectural Code Generation Tool
Accepts block level architectural input including third party IP and generates implementation roadmap by defining placeholders for all modules and interfaces

Fiesta® Process Standardization and Acceleration Tool Kit is an industrial strength suite of tools designed, developed, tested and used by engineers of Comit's Contract Engineering Center. Their experience in developing processes and methodology that yield predictable and accurate results forms the foundation of the toolkit. Use it with confidence.

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COMIT® SYSTEMS
The Contract Engineering Company

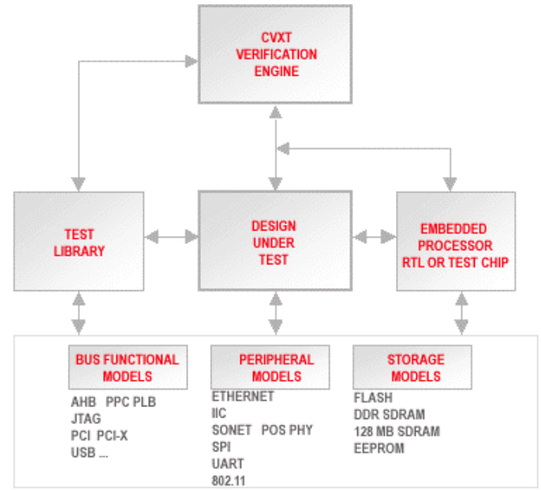
Fiesta® CVXT from Comit
Open Verification Environment

Fiesta® CVXT is a complete Open Verification Environment. It saves time by allowing rapid and painless implementation of module-interactive system level testing that is difficult to do in Verilog or C. Commonly available alternatives for system level verification require the designer to master an additional or proprietary syntax or language. In Fiesta® CVXT, tests are specified in Tcl using a set of just 12 commands. The CVXT Verification Engine provides the needed interactivity between tests and models to simulate a real-world environment.

Fiesta® CVXT offers the ability to build parallel, automated, synchronized self-checking verification testbenches for complex ASIC, SoC and programmable SoC designs. The environment bolts on to industry standard Verilog simulators and supports both real-world system testing and rigorous hardware module level and interface tests. The user can either run system level code intended for final silicon to test functionality, or do feature-by-feature self-checking of the chip modules, in parallel and in simultaneous interaction with other modules in the design.

Benefits

- Easy adoption due to open Tcl based environment
- Speeds up verification by automating real-world fully parallel testing
- Multiple test modes allows easy verification of design intent or rigorous checking of modules and interfaces
- Speedy testing of different prototypes provide rapid feedback for architecture adjustments
- Quickly tests different embedded processors by changing testchips and Bus Functional Models (BFM)
- Highly automated environment makes it convenient to run self-checking tests
- Completely scripted - requires no recompilation or elaboration, allowing for rapid changes



Key Features

- Sophisticated Verification Engine connects Verification Workbench to user-defined testbenches
  - Uses existing Verilog/C models
  - Supports industry standard Verilog simulators
  - Tests accuracy of modules and interfaces at the RTL level
  - Synchronizes tests with each other and with the simulator
  - Runs test in parallel and in simultaneous interaction with other modules in the design
  - Supports infinite number of parallel tests with independent execution contexts
  - Supports feature-by-feature self checking of modules
  - Supports if-then-else, events and triggers
  - Automatically waits for events and triggers from other interfaces
  - Supports top-down test-my-chip or bottom-up check-all-modules-and-interfaces mode
  - Supports execution of system level code to check functional intent
- DUT Socket architecture enables easy testing of multiple prototypes
- Testchip Socket enables plugging in of embedded processor testchips
- Wrapper architecture supports integration of user defined and third party BFM and peripheral models from expandable model library
- Model library supports BFM and peripheral models