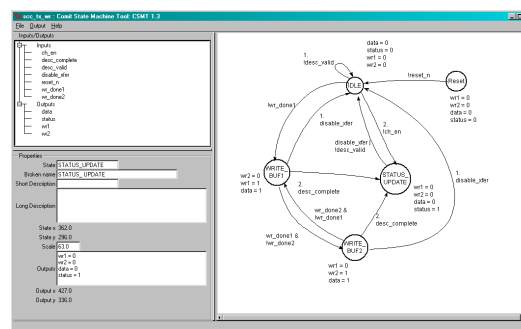


Fiesta[®] CSMT from Comit Finite State Machine Editor

Fiesta[®] CSMT is a graphical editor for finite state machines. This tool saves time by allowing rapid and easy definition of state machines and automatically generating Verilog[®] code and documentation. The tool provides a Graphical User Interface (GUI) that lets users add states, transitions, expressions, input and output signals to a state machine. The GUI provides easy drawing of state machine diagrams.

Benefits

- Intuitive Graphical User Interface speeds adoption
- Saves time by automatically generating Verilog code, diagrams and documentation
- Speeds up design realization time by automatically detecting errors
- Minimizes overhead by integrating directly with version control / release management tools
- Saves design debug time by automatically embedding entity descriptions in tool outputs



Key Features

- Easy to use Graphical User Interface
- Automatically generates Verilog HDL code
- Automatically generates diagrams in Postscript and Window Metafile formats
- Direct integration into version control/release management tools like cvs and make
- Built in Design Rule Check
- Automatically embeds entity description as comments in verilog code
- Automatically includes entity description in documentation

Specifications

Inputs

- Via GUI

Outputs

- Verilog code for state machine
- State machine diagram: .PS, .WMF
- Diagrams and Tables: .HTML, .RTF

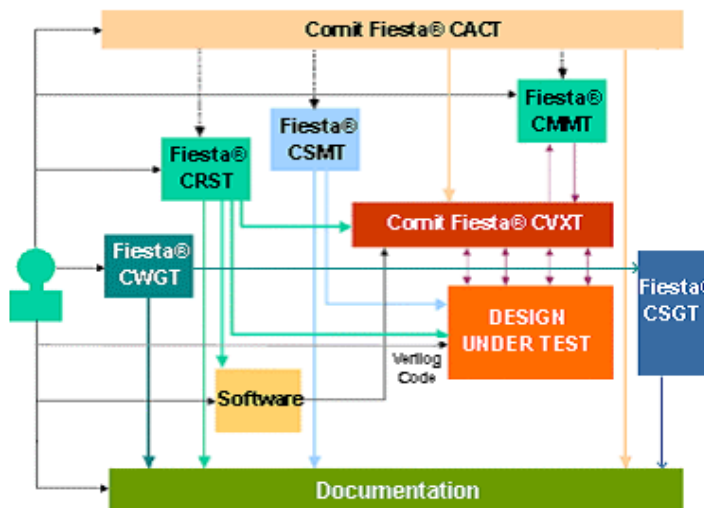
Platforms

OS	Ver.
Solaris (Sparc)	2.7
Windows NT	4.0
Red Hat Linux	7.1

Comit Fiesta® CSMT is part of the Comit Fiesta® Process Standardization & Acceleration Toolkit. Individual tools are designed to work in standalone mode or in cascade, where the output of one tool can be used by another.

Fiesta® Process Standardization & Acceleration Toolkit is an integrated set of tools with a vision to painlessly transform specification to product, by producing as much of code and documentation automatically as possible, and simultaneously setting up a compatible verification environment from the start. Designers, therefore, are free to focus on designing state machines and creating tests. Coexists with industry standard EDA tools for simulation, synthesis and layout.

The toolkit consists of the following additional tools:



Fiesta® CRST Register Specification Tool

Accepts register bank definitions for a chip. Generates and regenerates documentation, software interface definitions, hardware implementations and verification definitions, preserving consistency, and avoiding errors

Fiesta® CVXT Open Verification Environment

Provides the ability to build parallel, automated, synchronized, self-checking verification testbenches for complex ASIC, SoC and programmable SoC designs. The environment bolts on to industry standard Verilog simulators and supports both real-world system testing and rigorous hardware module level and interface tests

Fiesta® CMMT Simulation Memory Modeler

Generates dynamically configurable simulation time memory models that can be used in advanced system-level verification

Fiesta® CSGT Synthesis Script Generator

Accepts constraints and generates script to automate synthesis flow for popular synthesis tools

Fiesta® CAVT AHDL to VHDL Conversion tool

Converts Altera's proprietary HDL - AHDL to portable VHDL files to target any technology

Fiesta® CWGT Waveform Generation Tool

Produces output signal waveforms based on a GUI based input of signals and their transitions.

Fiesta® CACT Architectural Code Generation Tool

Accepts block level architectural input including third party IP and generates implementation roadmap by defining placeholders for all modules and interfaces.

Fiesta® Process Standardization and Acceleration Tool Kit is an industrial strength suite of tools designed, developed, tested and used by engineers of Comit's Contract Engineering Center. Their experience in developing processes and methodology that yield predictable and accurate results forms the foundation of the toolkit. Use it with confidence.

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**Comit Systems, Inc. 3375 Scott Blvd. Ste 139, Santa Clara, CA 95054.
(408) 988 2988. www.comit.com**