Fiesta® CSGT from Comit
Synthesis Script Generation Tool

Fiesta® CSGT is an ASIC synthesis script generation tool targeting Synopsys® synthesis tools. CSGT provides an intuitive graphical user interface, so that the user need not remember and use the synthesis tool commands.

Fiesta® CSGT automates creation of synthesis scripts. The tool reads a set of existing hierarchical Verilog® design files. Design attributes like clocks, port signals are automatically inferred and need not be specified by the user. The user is prompted for the relevant constraints. The tool can generate synthesis scripts for the entire design or for selected modules.

Benefits

- Intuitive Graphical User Interface promotes easy adoption and integration into design cycle
- Includes a design hierarchy browser
- Automatically infers clocks and other port characteristics
- Saves the project files for reuse
- User does not need to remember all the design compiler commands and options
- Forms ask all relevant constraint questions, reducing constraint omissions
- Automatic generation of scripts for Synopsys® Design Compiler.

Key Features

- Intuitive Graphical User Interface
- Web based tool
- Reads existing hierarchical Verilog designs.
- Detects system clocks and ports
- Provides complete design setup and compile options constraints
- Generates script for all the modules in the design
- Selective script generation

Specifications

Inputs

- Verilog design files
- GUI based options and constraints
- Text constraint file

Outputs

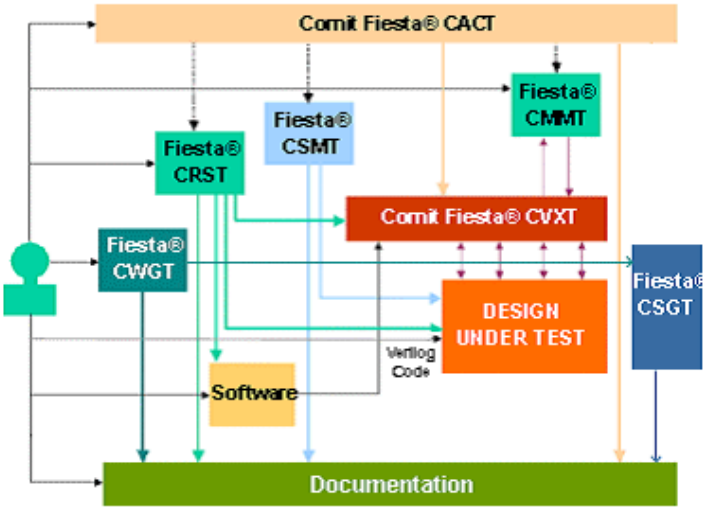
- Scripts for Synopsys® Design Compiler tool

Platforms

Platform Independent. Web browsers supporting JDK 1.3

Comit Fiesta® CSGT is part of the Comit Fiesta® Process Standardization & Acceleration Toolkit. Individual tools are designed to work in standalone mode or in cascade, where the output of one tool can be used by another.

Fiesta® Process Standardization & Acceleration Toolkit is an integrated set of tools with a vision to painlessly transform specification to product, by producing as much of code and documentation automatically as possible, and simultaneously setting up a compatible verification environment from the start. Designers, therefore, are free to focus on designing state machines and creating tests. Coexists with industry standard EDA tools for simulation, synthesis and layout.



The toolkit consists of the following additional tools:

Fiesta® CACT Architectural Code Generation Tool
Accepts block level architectural input including third party IP and generates implementation roadmap by defining placeholders for all modules and interfaces.

Fiesta® CWGT Waveform Generation Tool
Produces output signal waveforms based on a GUI based input of signals and their transitions.

Fiesta® CRST Register Specification Tool
Accepts register bank definitions for a chip. Generates and regenerates documentation, software interface definitions, hardware implementations and verification definitions, preserving consistency, and avoiding errors

Fiesta® CSMT Finite State Machine Editor
Generates synthesizable Verilog code, and diagrams for documentation from state machines.

Fiesta® CVXT Open Verification Environment
Provides the ability to build parallel, automated, synchronized self-checking verification testbenches for complex ASIC, SoC and programmable SoC designs. The environment bolts on to industry standard Verilog simulators and supports both real-world system testing and rigorous hardware module level and interface tests.

Fiesta® CMMT Simulation Memory Modeler
Generates dynamically configurable simulation time memory models that can be used in advanced system-level verification.

Comit Fiesta® Process Standardization and Acceleration Toolkit has been developed in close collaboration with practising design engineers at Comit's Silicon Valley Contract Engineering Center, and has been field-proven by them to deliver real-life multi-million-gate FPGA and deep sub-micron SoC designs. Comit's expertise in developing design process methodologies that yield predictable, accurate results forms the foundation of the toolkit.

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