COMIT® SYSTEMS
The Contract Engineering Company

Fiesta® CRST from Comit
Register Specification Tool

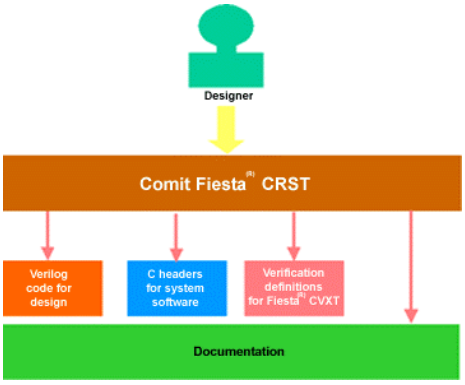
Fiesta® CRST is a register specification and change management tool. Manual definition of register specifications is time consuming and error-prone. Specification changes introduce further delays and increase the probability of errors due to the need for rewriting Verilog code and redoing documentation. Propagation of changes is hard to track manually.

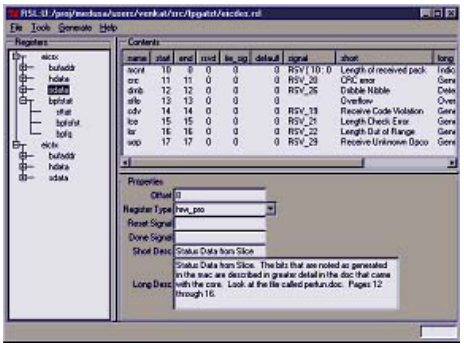
Fiesta® CRST aids design implementation by automating the specification of registers. It automatically generates the necessary synthesizable Verilog code, verification definitions that plug into Fiesta® Open Verification Environment, C headers and documentation, dramatically speeding up design, verification and software development cycles and updating documentation, all at one go. The tool automatically propagates specification changes to all generated outputs, ensuring consistency, and further reducing the possibility of errors.

Designers will start using the tool during the micro-architecture and design phase. Changes can be easily made to the registers, with all outputs automatically regenerated. Device driver development can start as soon as the first cut register specification is done, allowing for early feedback loops.

Benefits

- Intuitive Graphical User Interface promotes easy adoption and integration into design cycle
- Automatic input validations reduce errors
- Automatic generation and regeneration of directly synthesizable Verilog code dramatically compresses design cycle
- Automatic generation and regeneration of design document reduces time spent in documentation
- Automatic generation and regeneration of C headers reduces software development time
- Automatic generation and regeneration of register information useful for verification reduces verification time: (in Tcl for Comit Fiesta® CVXT Open Verification Environment, or a parse-able text file)
- Direct integration into version control and release management tools like *cvs* and *make* supports version-compares
- Reusable Write-once Use-many bus interface library scheme helps build repository of reusable interface definitions





Key Features

- Intuitive Graphical User Interface
- Flexible options to define a variety of bus interface libraries
- Bus interface library reusability
- Generated Verilog code suitable for synthesis and simulation
- Professional documentation output: customizable heading levels and options suitable for inclusion into MS-Word documents
- Sample instantiation templates for generated modules
- Built-in design rule checks for automatic, early detection of specification inconsistencies
- Automatic filling for unused portions of registers
- Automatic documentation facilitates good design practice
- Data format directly compatible with version control and release management tools

Specifications

Inputs

- GUI based specifications for registers

Outputs

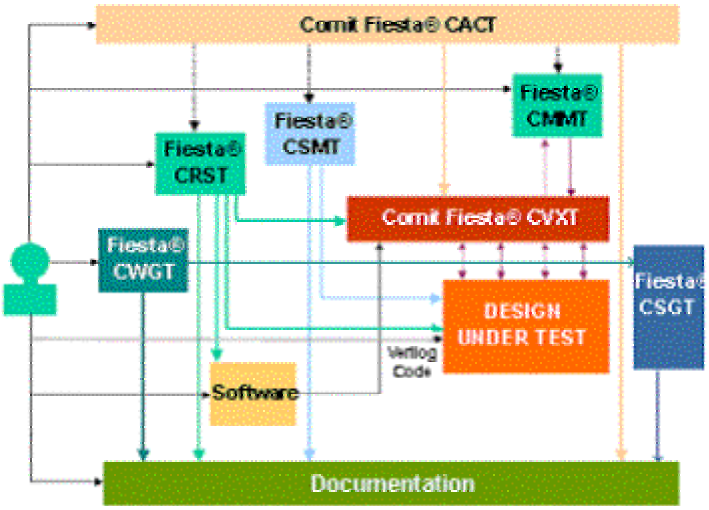
- Register bank with registers, Instantiation Template, Definitions (`defines) for easy use in other verilog sources: Verilog
- Header file definitions for each register and each bitfield - used for diagnostic software, and device driver development: C
- Verification definitions, for Comit Fiesta® CVXT, automated register read write, power up and reset tests: Tcl
- Documentation in MS-Word

Platforms

OS	Version
Solaris (Sparc)	2.7
Linux	Redhat 7.1
Windows NT	4.0
Windows 95/98/ME	All
Windows 2000/XP	All

Comit Fiesta® CRST is part of the Comit Fiesta® Process Standardization & Acceleration Toolkit. Individual tools are designed to work in standalone mode or in cascade, where the output of one tool can be used by another.

Fiesta® Process Standardization & Acceleration Toolkit is an integrated set of tools with a vision to painlessly transform specification to product, by producing as much of code and documentation automatically as possible, and simultaneously setting up a compatible verification environment from the start. Designers, therefore, are free to focus on designing state machines and creating tests. Coexists with industry standard EDA tools for simulation, synthesis and layout.



The toolkit consists of the following additional tools:

Fiesta® CVXT Open Verification Environment
Provides the ability to build parallel, automated, synchronized, self-checking verification testbenches for complex ASIC, SoC and programmable SoC designs. The environment bolts on to industry standard Verilog simulators and supports both real-world system testing and rigorous hardware module level and interface tests

Fiesta® CSMT Finite State Machine Editor
Generates synthesizable Verilog code, and diagrams for documentation from state machines.

Fiesta® CMMT Simulation Memory Modeler
Generates dynamically configurable simulation time memory models that can be used in advanced system-level verification

Fiesta® CSGT Synthesis Script Generator
Accepts constrains and generates script to automate synthesis flow for popular synthesis tools

Fiesta® CAVT AHDL to VHDL Conversion tool
Converts Altera's proprietary HDL - AHDL to portable VHDL files to target any technology

Fiesta® CWGT Waveform Generation Tool
Produces output signal waveforms based on a GUI based input of signals and their transitions.

Fiesta® CACT Architectural Code Generation Tool
Accepts block level architectural input including third party IP and generates implementation roadmap by defining placeholders for all modules and interfaces

Fiesta® Process Standardization and Acceleration Tool Kit is an industrial strength suite of tools designed, developed, tested and used by engineers of Comit's Contract Engineering Center. Their experience in developing processes and methodology that yield predictable and accurate results forms the foundation of the toolkit. Use it with confidence.

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