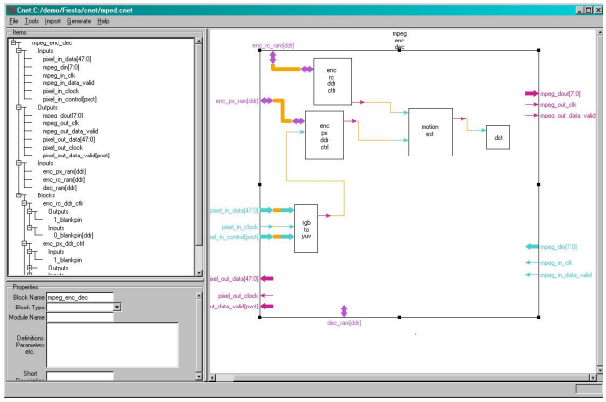
COMIT® SYSTEMS
The Contract Engineering Company

Fiesta® CACT from Comit Architecture Capture Tool

Fiesta® CACT is a VLSI design tool for architecture definition, structural design and code generation. Its graphical editor allows designers to input block level architecture, including third party IP, and generate an implementation roadmap for all modules and interfaces. The tool saves time by allowing rapid and easy definition of architectural blocks and automatically generating Verilog® and VHDL code and documentation. The Graphical User Interface (GUI) lets users add blocks in a hierarchical manner. CACT also generates system and module level block diagrams with the ability to automatically connect signals by name. CACT also makes drawing block diagrams a breeze.

Benefits

- Intuitive Graphical User Interface speeds adoption
- Can use graphical input or existing code as starting point.
- Generates HDL code, professional diagrams and organized documentation
- Minimizes overhead by integrating directly with version control / release management tools
- Saves design debug time by automatically embedding entity descriptions in tool outputs
- Makes explanation and understanding time, especially for code reviews, for code maintenance and transfer of technology.
- Guarantees consistency between documentation and code.
- Eliminates redundant information entry.



Key Features

- Easy to use Graphical User Interface enables definition of connectivity as well as properties and comments for design elements.
- Bus definitions enable non-cluttered schematics, even at ASIC top levels.
- Imports HDL code, and infers connectivity and hierarchy information, making it easy to use the tool for existing code and for third party IP.
- Automatically generates fully commented Verilog® or VHDL code. Comments include connectivity information, making debug easier.
- Automatically generates professional looking vectored diagrams in Postscript and Windows™ Metafile formats, including complete MS-Word® documentation including inline diagrams.
- Automatically generates pin tables in generated documentation, reducing redundancy in user input.
- ASCII database makes it easy to integrate database into version control/release management tools like cvs and Perforce.

Specifications

Inputs

- Via GUI
- Import of Verilog® code

Outputs

- Verilog® code for modules
- Block diagram: .PS, .WMF
- Diagrams and Tables: .HTML, .RTF
- Complete Documentation in Word format.

Platforms

OS	Version
Solaris® (Sparc)	2.7/ 2.8 (7/ 8)
Windows™	NT 4.0 / 98 / 2000 / XP
Red Hat® Linux	7.1 / 7.2 (may work on other versions)

Comit Fiesta® CACT is the anchor tool of the Comit Fiesta® Process Standardization & Acceleration Toolkit, and connects to other tools in the chain. Individual tools are designed to work in standalone mode or in cascade, where the output of one tool can be used by another. Fiesta® CACT manages overall design project organization and handoff-elements between other tools in the toolkit.

Fiesta® Process Standardization & Acceleration Toolkit is an integrated set of tools with a vision to painlessly transform specification to product, by producing as much of code and documentation automatically as possible, and simultaneously setting up a compatible verification environment from the start. Designers, therefore, are free to focus on designing state machines and creating tests. Coexists with industry standard EDA tools for simulation, synthesis and layout.

The toolkit consists of the following additional tools:

Fiesta® CWGT Waveform Generation Tool
Produces output signal waveforms based on a GUI based input of signals and their transitions.

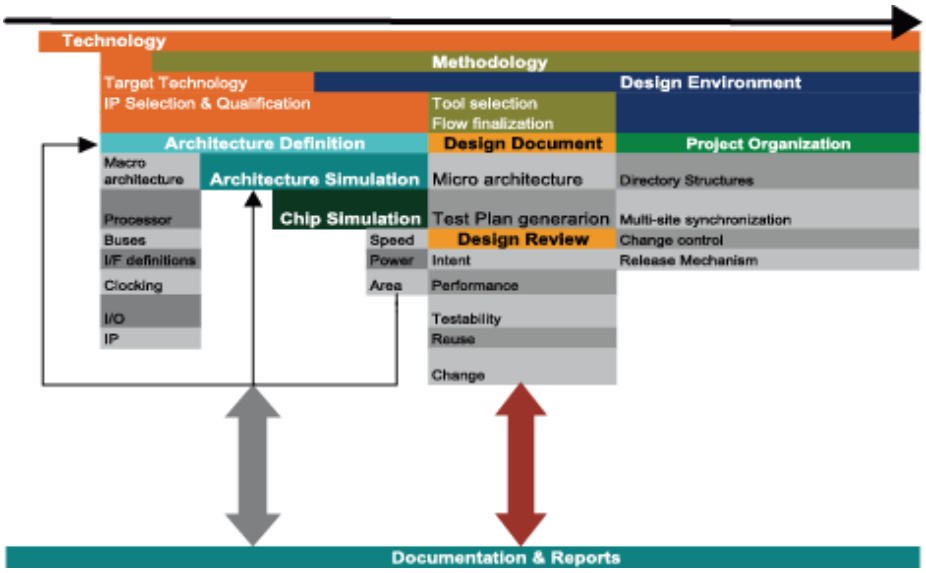
Fiesta® CRST Register Specification Tool
Accepts register bank definitions for a chip. Generates and regenerates documentation, software interface definitions, hardware implementations and verification definitions, preserving consistency, and avoiding errors

Fiesta® CSMT Finite State Machine Editor
Generates synthesizable Verilog® code, and diagrams for documentation from state machines.

Fiesta® CVXT Open Verification Environment
Provides the ability to build parallel, automated, synchronized, self-checking verification testbenches for complex ASIC, SoC and programmable SoC designs. The environment bolts on to industry standard Verilog® simulators and supports both real-world system testing and rigorous hardware module level and interface tests

Fiesta® CMMT Simulation Memory Modeler
Generates dynamically configurable simulation time memory models that can be used in advanced system-level verification

Fiesta® CSGT Synthesis Script Generator
Accepts constraints and generates script to automate synthesis flow for popular synthesis tools



Comit Fiesta® Process Standardization and Acceleration Toolkit has been developed in close collaboration with practising design engineers at Comit's Silicon Valley Contract Engineering Center, and has been field-proven by them to deliver real-life multi-million-gate FPGA and deep sub-micron SoC designs. Comit's expertise in developing design process methodologies that yield predictable, accurate results forms the foundation of the toolkit.

Comit Systems, Inc. 3375 Scott Blvd. Ste 139, Santa Clara, CA 95054.
(408) 988 2988. www.comit.com