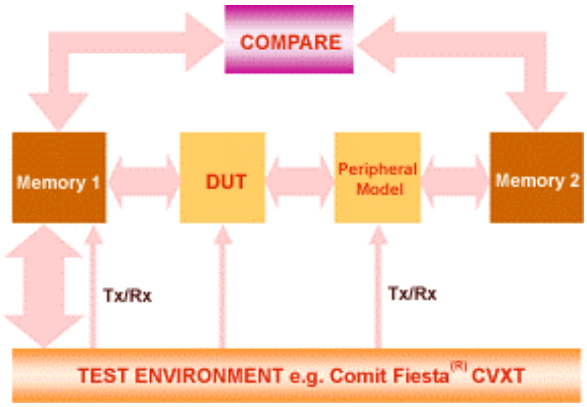
Fiesta® CMMT from Comit
Simulation Memory Modeler

Fiesta® CMMT is a tool to generate simulation time memory models that can be used in advanced system-level verification. Fiesta® CMMT can generate memories with built-in high-level task-definitions to facilitate access from the Comit Fiesta® CVXT Open Verification Environment or standalone Tcl test cases to set up and read data in blocks.

Fiesta® CMMT can configure memory models to any size. Width and depth are dynamically changeable at run time. Memory models generated can be used in test environments involving many interfaces like Ethernet, Voice (SCC), ADSL, HPNA, USB and their peripheral models in a test environment.

Benefits

- Easily set up and test interfaces needing large packet transfers
- Automatically compare transmit and receive data with easy PLI access
- Easily detect faults in compared data and debug interfaces
- Shorten verification cycles



Key Features

- Direct instantiation in the verification environment with different memory names
- Depth and width specification using PLI
- Initialization to desired values using PLI
- Maximum memory area limited only by simulator memory
- Can be used in Verilog and Tcl environments
- Memory can be read / written with simple commands (PLI), for example:
  $cmread (memory_name, address_to_be_read_from , register_to_be_stored_in)
  $cmwrite (memory_name, address_to_be_writen_to, data_reg)

Specifications
Inputs /Outputs

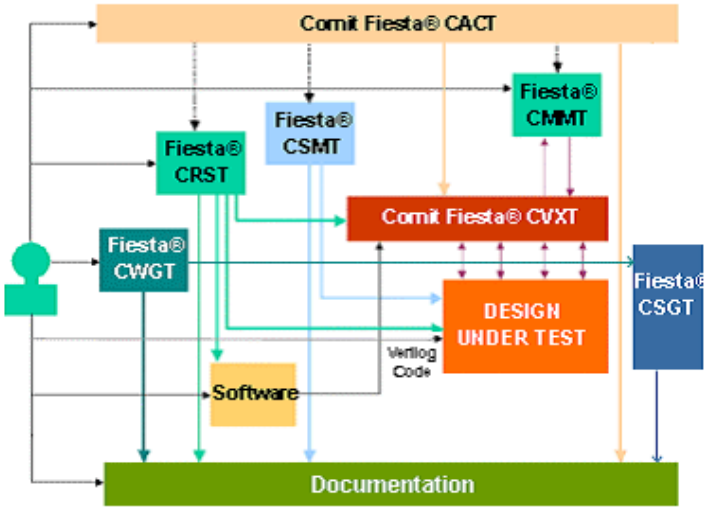
- Test bench (Comit Fiesta® CVXT or other Verilog/Tcl environment)
- Peripheral models

Environment
Verilog, Tcl, C

Comit Fiesta® CMMT is part of the Comit Fiesta® Process Standardization & Acceleration Toolkit. Individual tools are designed to work in standalone mode or in cascade, where the output of one tool can be used by another.

Fiesta® Process Standardization & Acceleration Toolkit is an integrated set of tools with a vision to painlessly transform specification to product, by producing as much of code and documentation automatically as possible, and simultaneously setting up a compatible verification environment from the start. Designers, therefore, are free to focus on designing state machines and creating tests. Coexists with industry standard EDA tools for simulation, synthesis and layout.

The toolkit consists of the following additional tools:



Fiesta® CRST Register Specification Tool
Accepts register bank definitions for a chip. Generates and regenerates documentation, software interface definitions, hardware implementations and verification definitions, preserving consistency, and avoiding errors

Fiesta® CVXT Open Verification Environment
Provides the ability to build parallel, automated, synchronized, self-checking verification testbenches for complex ASIC, SoC and programmable SoC designs. The environment bolts on to industry standard Verilog simulators and supports both real-world system testing and rigorous hardware module level and interface tests

Fiesta® CSMT Finite State Machine Editor
Generates synthesizable Verilog code, and diagrams for documentation from state machines.

Fiesta® CSGT Synthesis Script Generator
Accepts constrains and generates script to automate synthesis flow for popular synthesis tools

Fiesta® CAVT AHDL to VHDL Conversion tool
Converts Altera's proprietary HDL - AHDL to portable VHDL files to target any technology

Fiesta® CWGT Waveform Generation Tool
Produces output signal waveforms based on a GUI based input of signals and their transitions.

Fiesta® CACT Architectural Code Generation Tool
Accepts block level architectural input including third party IP and generates implementation roadmap by defining placeholders for all modules and interfaces.

Fiesta® Process Standardization and Acceleration Tool Kit is an industrial strength suite of tools designed, developed, tested and used by engineers of Comit's Contract Engineering Center. Their experience in developing processes and methodology that yield predictable and accurate results forms the foundation of the toolkit. Use it with confidence.

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