COMIT® SYSTEMS
The Contract Engineering Company

Fiesta® CMBT from Comit
Memory BIST Controller

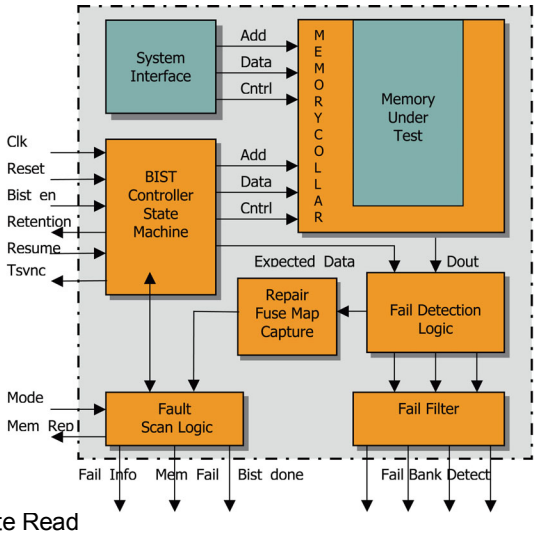
Fiesta® CMBT Memory BIST controller provides a complete solution for the **full speed testing** of embedded Random Access Memories developed and manufactured in advanced deep sub-micron silicon process technology. Fiesta® CMBT, with its full speed memory testing, reduces the risk of delay in product introduction, and speeds up time to market.

Full-speed testing, where **both the clock speed and access speeds are real life values**, is a precise method of testing on-chip memories, compared to at-speed testing where only the clock is real life, but access speeds are slower. Full-speed testing exercises memory for writes and reads with no back-to-back clock cycle delay, as contrasted with at-speed. At speed memory BIST may pass memory with no faults detected, but may fail on chip, when exercised by the real life logic at full speed.

Fiesta® CMBT tests memory at actual speed of access, ensuring accurate parts screening, minimizing shipment of bad parts and potential cost of wasted masks and material.

Benefits

- Full-speed testing catches more faults than other available controllers that test at-speed, reducing shipment of bad parts
- Dual-mode operation aids wafer-sort as well as debug and engineering
- Automatic fuse map generation for laser repair stations saves time and money
- Exhaustive test bench simulates memory faults and verifies controller algorithms
- Intuitive Graphical User Interface promotes easy adoption and integration into design cycle
- Automatic input validations reduce errors



Key Features

- Full speed memory BIST
- Handles memory write & read pipeline
  - Early write, Late write, Early read, Late-Late Read
- Detects following types of faults:
  - Stuck at faults, Stuck open faults
  - Coupling faults, Transition faults
  - Leakage Faults, Retention faults
- Two Modes of operation:
  - Wafer Sort
    - Pass/Fail, Serial shift of Fuse map for laser repair
  - Debug and Engineering for characterization
    - Serial output for faulty memory location's Address, Data and Fail state
- Automatic Fuse Map Information generation for Laser repair stations
- Individual Memory sector failure detection and indication
- Avoids multiple indication of same faulty location
- Instantiates memory collar
- Indicates whether memory is repairable or not
- Exhaustive test bench for
  - Fault insertion
  - Detection
  - Automatic data capture
  - Data comparison
- Verilog® / VHDL RTL and Test Bench generation
- Compatible with industry standard tools

Specifications

Inputs

- Via GUI

Outputs

- RTL
- Test bench
- Documentation
- Synthesis script

Platforms

OS	Version
Solaris® (Sparc)	2.7 / 2.8 (7 / 8)
Red Hat® Linux	7.1

Fiesta® CMBT is the latest addition to the Comit Fiesta® Process Standardization and Acceleration Toolkit. Fiesta® has been developed in close collaboration with practicing design engineers at Comit's Silicon Valley Contract Engineering Center, and has been field-proven by them to deliver real-life multi-million-gate FPGA and deep sub-micron SoC designs. Comit's expertise in developing design process methodologies that yield predictable, accurate results forms the foundation of the toolkit.

Comit Systems, Inc. 3375 Scott Blvd. Ste 139, Santa Clara, CA 95054.
(408) 988 2988. www.comit.com